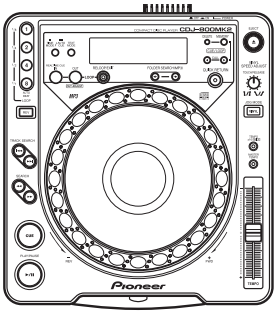
Pioneer *sound.vision.soul*

Service Manual



CDJ-800MK2

ORDER NO.
RRV3364

COMPACT DISC PLAYER

CDJ-800MK2

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Model	Type	Power Requirement	Remarks
CDJ-800MK2	KUCXJ	AC 120 V	
CDJ-800MK2	WYXJ5	AC 220 – 240 V	
CDJ-800MK2	RLFXJ	AC 110-120 V / 220-240 V	

For details, refer to "Important symbols for good services" .

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ⓒ**PIONEER CORPORATION 2006**

T-ZZR JUNE 2006 printed in Japan

SAFETY INFORMATION

This service manual is intended for qualified service technicians ; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.
Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING
This product contains lead in solder and certain electrical parts contain chemicals which are known to the state of California to causecancer, birth defects or other reproductive harm.

Health & Safety Code Section 25249.6 – Proposition 65

NOTICE
(FOR CANADIAN MODEL ONLY)
Fuse symbols (fast operating fuse) and/or (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

REMARQUE
(POUR MODÈLE CANADIEN SEULEMENT)
Les symboles de fusible (fusible de type rapide) et/ou (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

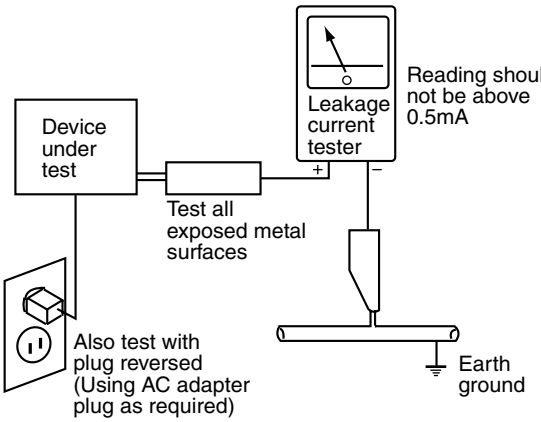
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (waterpipe , conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.


Device under test
Leakage current tester
Reading should not be above 0.5mA
+
–
Test all exposed metal surfaces
Also test with plug reversed (Using AC adapter plug as required)
Earth ground

AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which does not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

IMPORTANT

THIS PIONEER APPARATUS CONTAINS LASER OF CLASS 1.
SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUCTED PERSON.

LASER DIODE CHARACTERISTICS

MAXIMUM OUTPUT POWER: 5 mW
WAVELENGTH: 780 – 785 nm

WARNING !

The AEL(accessible emission level) of the laser power output is less then **CLASS 1** but the laser component is capable of emitting radiation exceeding the limit for **CLASS 1.**

A specially instructed person should servicing operation of the apparatus.

LABEL CHECK

CDJ-800MK2 WYXJ5 and KUCXJ : Types Only

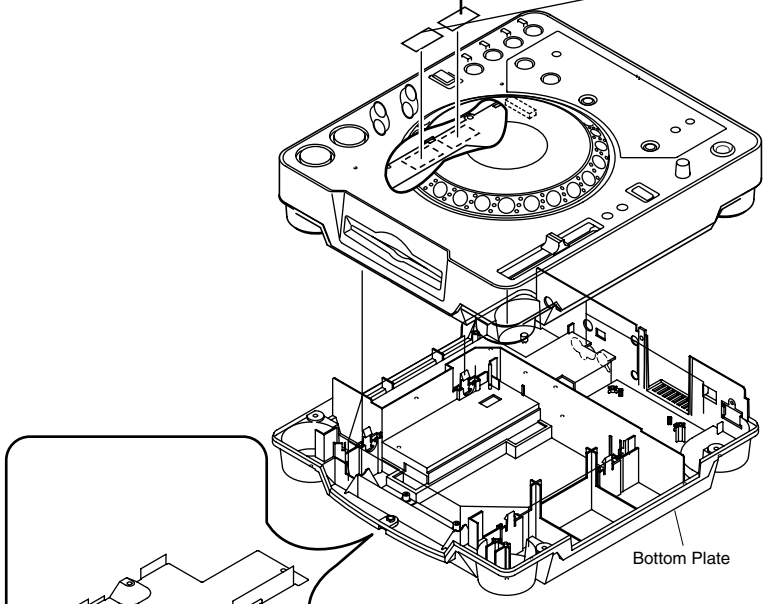
CAUTION
CLASS 3B INVISIBLE LASER RADIATION WHEN OPEN. AVOID EXPOSURE TO BEAM.
ATTENTION
RADIATIONS LASER INVISIBLES DE CLASSE 3B QUAND OUVERT. EVITEZ TOUT EXPOSITION AU FAISCEAU.
ADVARSEL
KLASSE 3B USYNLIG LASERSTRÅLING VED ÅBNING. UNDGÅ UDSÆTTELSE FOR STRÅLING.
VARNING
KLASS 3B OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD. UNDVIK ATT UTSÄTTA DIG FÖR STRÅLEN
VORSICHT
BEI GEÖFFNETER ABDECKUNG IST UNSICHTBARE LASERSTRAHLUNG DER KLASSE 3B IM GERÄTEINNEREN VORHANDEN. NICHT DEM LASERSTRAHL AUSSETZEN!
PRECAUCIÓN
CUANDO SE ABRE HAY RADIACIÓN LÁSER DE CLASE 3B INVISIBLE. EVITE LA EXPOSICION A LOS RAYOS LÁSER.
VARO!
AVATTAESSA OLET ALTTIINA NÄKYMÄTTÖMÄLLE LUOKAN 3B LASERSÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN.
DRW2308-A

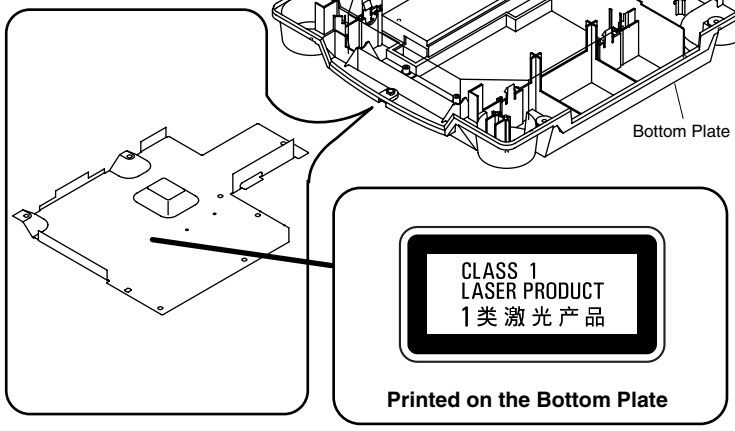
(DRW2308)

for RLFXJ

CAUTION : CLASS 3B INVISIBLE LASER RADIATION WHEN OPEN, AVOID EXPOSURE TO THE BEAM.
注意 : 打開時會有 CLASS 3B 不可見雷射輻射，請勿受雷射束輻射。
DRW2248

(DRW2248)





Printed on the Bottom Plate

Additional Laser Caution

1. Laser Interlock Mechanism
   The position of the switch (S1901) for detecting loading completion is detected by the system microprocessor, and the design prevents laser diode oscillation when the switch is not in LPS1 terminal side (when the mechanism is not clamped and LPS1 signal is high level.)
   Thus, the interlock will no longer function if the switch is deliberately set to LPS1 terminal side. (if LPS1 signal is low level).
   In the test mode* the interlock mechanism will not function. Laser diode oscillation will continue, if pin 41 of TC94A15FG (IC101) on the MAIN Assy is connected to GND, or else the terminals of Q101 are shorted to each other (fault condition).

2. When the cover is opened, close viewing of the objective lens with the naked eye will cause exposure to a Class 1 laser beam.

* : Refer to page 86.

[Important Check Points for Good Servicing]

In this manual, procedures that must be performed during repairs are marked with the below symbol.
Please be sure to confirm and follow these procedures.

1. Product safety

Please conform to product regulations (such as safety and radiation regulations), and maintain a safe servicing environment by following the safety instructions described in this manual.

① Use specified parts for repair.

Use genuine parts. Be sure to use important parts for safety.

② Do not perform modifications without proper instructions.

Please follow the specified safety methods when modification(addition/change of parts) is required due to interferences such as radio/TV interference and foreign noise.

③ Make sure the soldering of repaired locations is properly performed.

When you solder while repairing, please be sure that there are no cold solder and other debris.
Soldering should be finished with the proper quantity. (Refer to the example)

④ Make sure the screws are tightly fastened.

Please be sure that all screws are fastened, and that there are no loose screws.

⑤ Make sure each connectors are correctly inserted.

Please be sure that all connectors are inserted, and that there are no imperfect insertion.

⑥ Make sure the wiring cables are set to their original state.

Please replace the wiring and cables to the original state after repairs.
In addition, be sure that there are no pinched wires, etc.

⑦ Make sure screws and soldering scraps do not remain inside the product.

Please check that neither solder debris nor screws remain inside the product.

⑧ There should be no semi-broken wires, scratches, melting, etc. on the coating of the power cord.

Damaged power cords may lead to fire accidents, so please be sure that there are no damages.
If you find a damaged power cord, please exchange it with a suitable one.

⑨ There should be no spark traces or similar marks on the power plug.

When spark traces or similar marks are found on the power supply plug, please check the connection and advise on secure connections and suitable usage. Please exchange the power cord if necessary.

⑩ Safe environment should be secured during servicing.

When you perform repairs, please pay attention to static electricity, furniture, household articles, etc. in order to prevent injuries.
Please pay attention to your surroundings and repair safely.

2. Adjustments

To keep the original performance of the products, optimum adjustments and confirmation of characteristics within specification.
Adjustments should be performed in accordance with the procedures/instructions described in this manual.

3. Lubricants, Glues, and Replacement parts

Use grease and adhesives that are equal to the specified substance.
Make sure the proper amount is applied.

4. Cleaning

For parts that require cleaning, such as optical pickups, tape deck heads, lenses and mirrors used in projection monitors, proper cleaning should be performed to restore their performances.

5. Shipping mode and Shipping screws

To protect products from damages or failures during transit, the shipping mode should be set or the shipping screws should be installed before shipment. Please be sure to follow this method especially if it is specified in this manual.

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1. SPECIFICATIONS

Specifications

• KUCXJ type

1. General

System.....Compact disc digital audio system
Power requirements.....AC 120 V, 60 Hz
Power consumption.....20 W
Operating temperature..... +5˚C to +35˚C (+41˚F to +95˚F)
Operating humidity.....5 % to 85 %
(There should be no condensation of moisture.)
Weight.....4.0 kg (8.8 lb)
Dimensions..... 305 (W) × 344.1 (D) × 106.5 (H)mm
12 (W) × 13 –9/16 (D) × 4 – 1/4 (H) in

2. Audio section

Frequency response.....4 Hz to 20 kHz
Signal-to-noise ratio.....115 dB or more (JEITA)
Distortion..... .0.006 % (JEITA)

3. Accessories

• Operating instructions.....1
• Power cord.....1
• Audio cable..... 1
• Control cable..... 1
• Forced eject pin (housed in a groove in the bottom panel)... 1
• Limited warranty.....1

NOTE:
Specifications and design are subject to possible modification with-out notice.

• WYXJ5 type

1. General

System..... Compact disc digital audio system
Power requirements ..... AC 220-240 V, 50/60 Hz
Power consumption ..... 22 W
Operating temperature ..... +5°C to +35°C
Operating humidity ..... 5 % to 85 %
(There should be no condensation of moisture.)
Weight ..... 4.0 kg
Dimensions .....305 (W) x 344.1 (D) x 106.5 (H) mm

2. Audio section

Frequency response..... 4 Hz to 20 kHz
Signal-to-noise ratio ..... 115 dB or more (JEITA)
Distortion ..... 0.006 % (JEITA)

3. Accessories

• Operating instructions 1
• Power cord 1
• Audio cable 1
• Control cable 1
• Forced eject pin (housed in a groove in the bottom panel)... 1

NOTE:
Specifications and design are subject to possible modification with-out notice.

• RLFXJ type

1. General

System..... Compact disc digital audio system
Power requirements .... AC 110-120 V/220-240 V, 50/60 Hz
Power consumption ..... 22 W
For Taiwan: 21 W
Operating temperature .....+5°C to +35°C
Operating humidity ..... 5 % to 85 %
(There should be no condensation of moisture.)
Weight .....4.0 kg
Dimensions ..... 305 (W) x 344.1 (D) x 106.5 (H) mm

2. Audio section

Frequency response..... 4 Hz to 20 kHz
Signal-to-noise ratio ..... 115 dB or more (JEITA)
Distortion ..... 0.006 % (JEITA)

3. Accessories

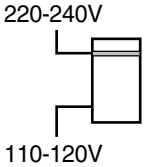
• Operating instructions 1
• Power cord 1
• Audio cable 1
• Control cable 1
• Forced eject pin (housed in a groove in the bottom panel)... 1

NOTE:
Specifications and design are subject to possible modification with-out notice.

Voltage selector (RLFXJ type only)

• You can find the voltage selector switch on the bottom plate of the unit.
The factory setting for the voltage selector is 220 – 240 V. Please set it to the correct voltage for your country or region.

• For Taiwan, please set to 110 – 120 V before using.
Before changing the voltage, disconnect the AC power cord. Use a medium size screwdriver to change the voltage selector switch.

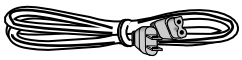


Accessories

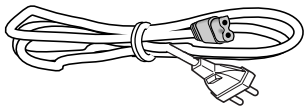
Audio Cable
(VDE1064) L=1.5m

Control Cord
(XDE3063) L=1 m

Power Cord
(ADG7021 : KUCXJ)
(ADG7097 : RLFXJ)



(ADG1154 : WYXJ,RLFXJ)

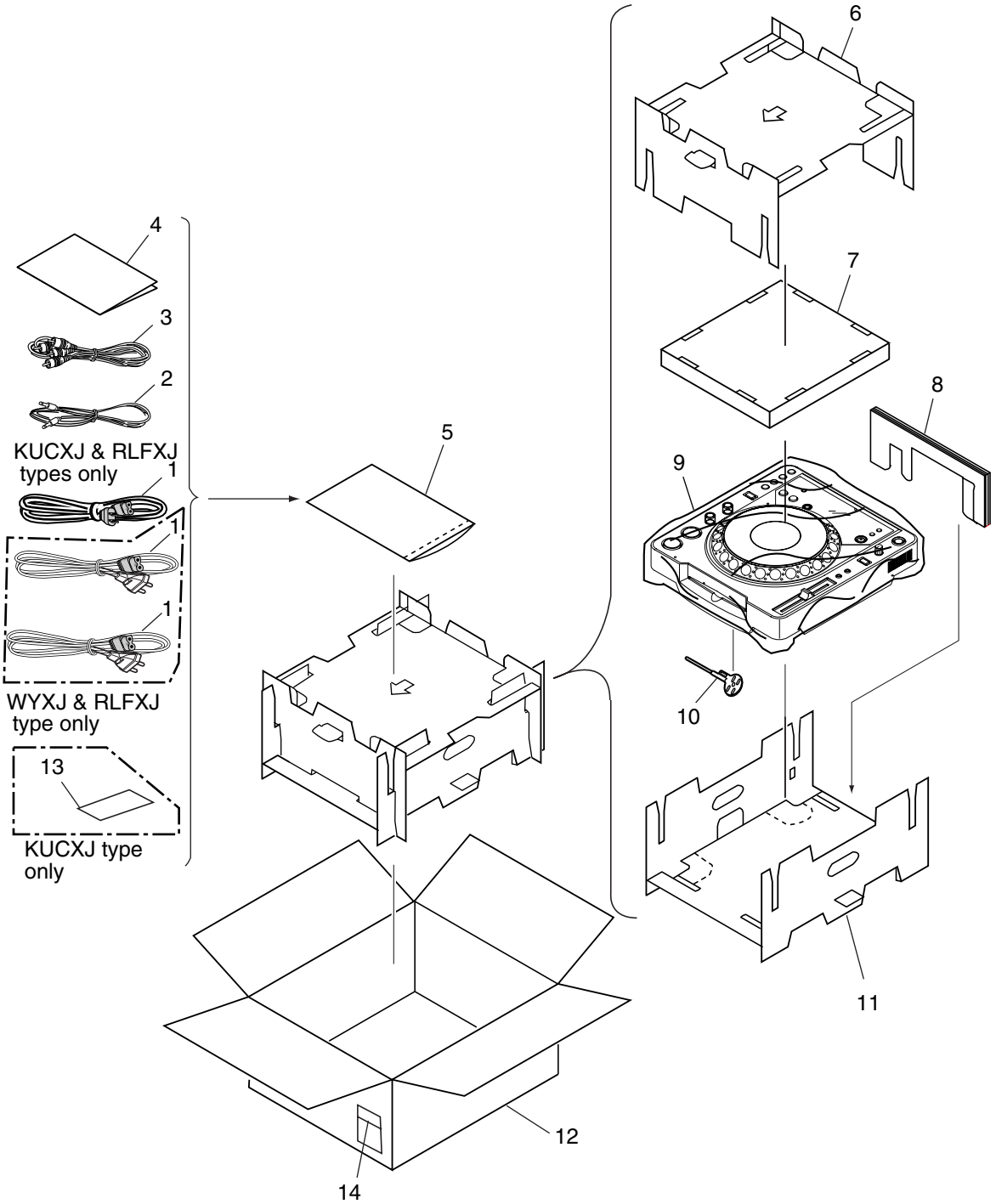


Forced Fject Pin
(housed in a groove in
the bottom panel)
(DEX1008)

2. EXPLODED VIEWS AND PARTS LIST

NOTES:
- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Screws adjacent to ▼ mark on product are used for disassembly.*
- *For the applying amount of lubricants or glue, follow the instructions in this manual. (In the case of no amount instructions, apply as you think it appropriate.)*

2.1 PACKING



PACKING parts List

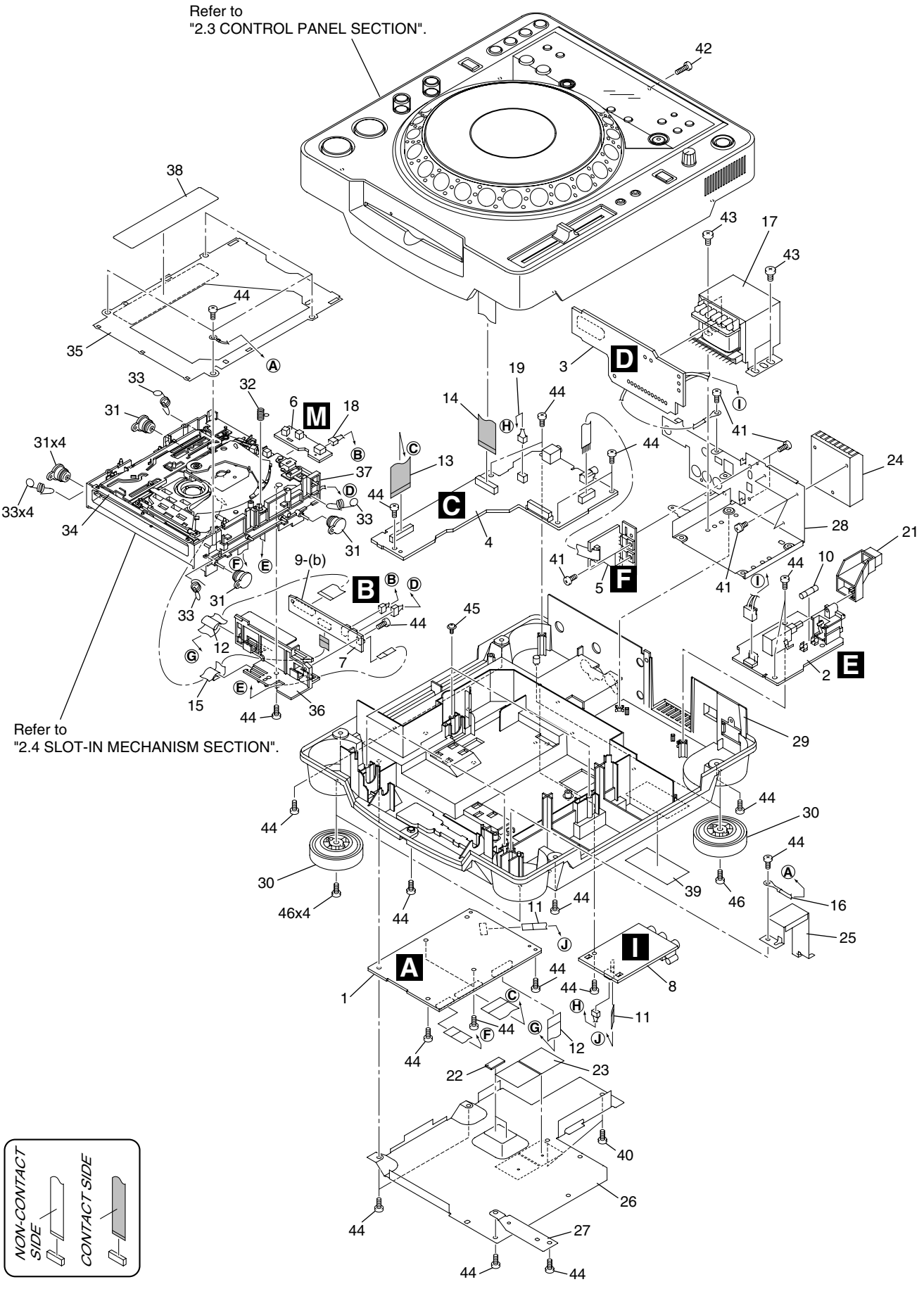
Mark	No.	Description	Part No.
⚠	1	AC Power Cord	See Contrast table(2)
	2	Control Cord	XDE3063
	3	Audio Cord	VDE1064
	4	Operating Instructions	See Contrast table(2)
NSP	5	Polyethylene Bag	AHG7117
	6	Pad B	DHA1556
	7	Pad C	DHA1557
	8	Pad D	DHA1558
	9	Sheet	RHX1006
	10	Push Rod	DEX1008
	11	Pad A	DHA1555
	12	Packing Case	See Contrast table(2)
NSP	13	Warranty Card	See Contrast table(2)
NSP	14	Label	See Contrast table(2)

(2) CONTRAST TABLE

CDJ-800MK2/KUCXJ, /WYXJ5 and RLFXJ types are constructed the same except for the following:

Mark	No.	Symbol and Description	CDJ-800MK2/ KUCXJ	CDJ-800MK2/ WYXJ5	CDJ-800MK2/ RLFXJ
⚠	1	AC Power Cord	ADG7021	ADG1154	ADG1154
⚠	1	AC Power Cord	Not used	Not used	ADG7097
	4	Operating Instructions (English)(KUCXJ)	DRB1401	Not used	Not used
	4	Operating Instructions (WYXJ5)(English, French, German, Italian, Dutch, Spanish)	Not used	DRB1400	Not used
	4	Operating Instructions (RLFXJ) (English, Spanish, Chinese)	Not used	Not used	DRB1402
	12	Packing Case	DHG2595	DHG2594	DHG2596
NSP	13	Warranty Card	ARY7043	Not used	Not used
NSP	14	Label	DRW2311	VRW1629	VRW1629

2.2 EXTERIOR SECTION



EXTERIOR SECTION parts List

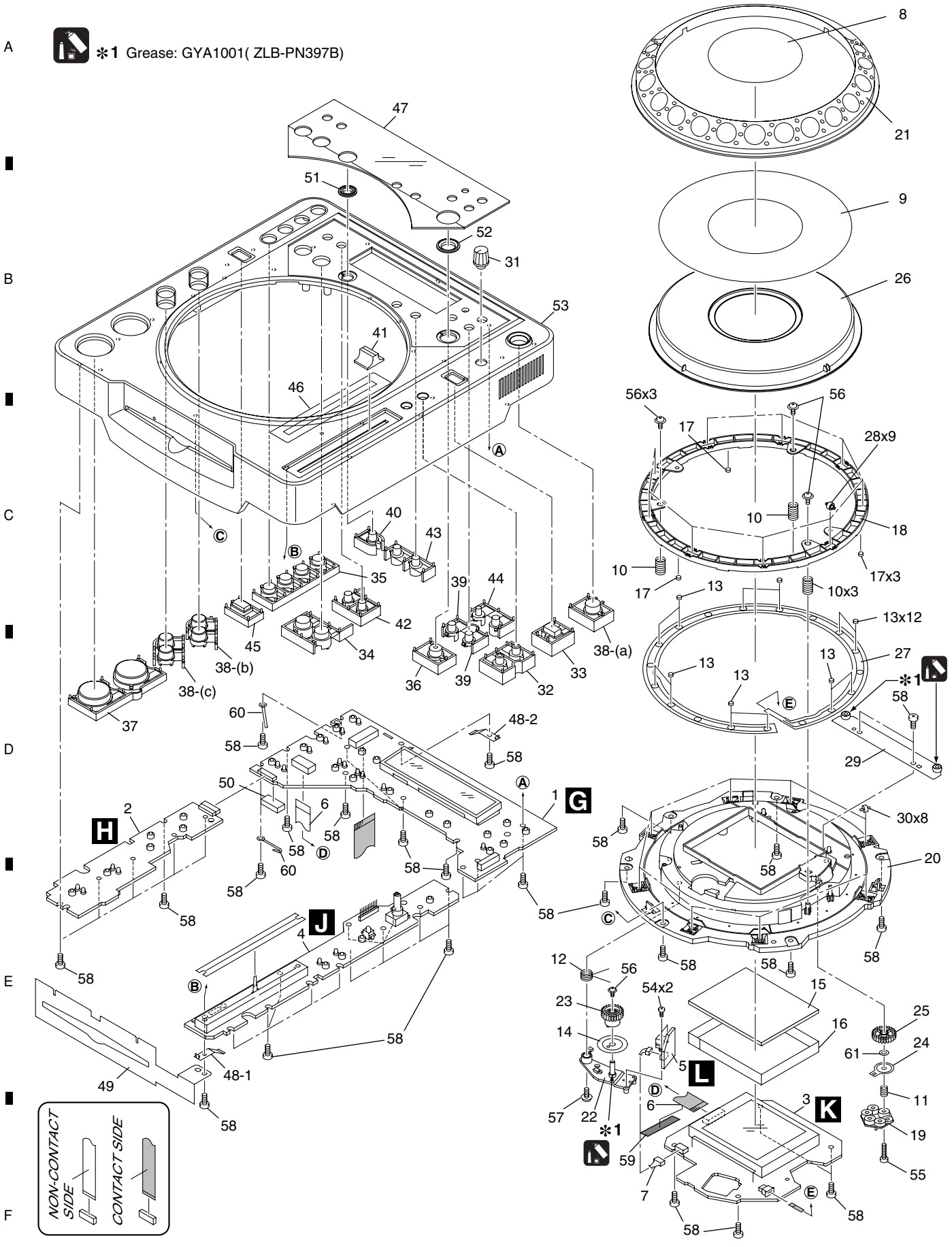
Mark	No.	Description	Part No.
	1	MAIN Assy	DWG1622
⚠	2	AC IN Assy	See Contrast table(2)
⚠	3	TRNS Assy	See Contrast table(2)
	4	SECB Assy	DWR1309
	5	REGB Assy	DWR1310
	6	SLMB Assy	DWS1388
	7	RLYB Assy	DWX2602
	8	JACK Assy	DWG1626
	9	• • • •	
⚠	10	Fuse	See Contrast table(2)
	11	FFC (9p)	DDD1311
	12	FFC (32p)	DDD1312
	13	FFC (25p)	DDD1313
	14	FFC (17p)	DDD1314
	15	FFC (24p)	DDD1315
NSP	16	Earth Lead	DE010VF0
⚠	17	Power Transfomer	See Contrast table(2)
	18	Connector Assy	PF03PP-B05
	19	Connector Assy	PF03PP-C12
	20	• • • •	
	21	Power Knob	DAC2073
NSP	22	Silicon Lubber D5 L	DEB1456
	23	Bottom Cushion S4	DEC2506
	24	Heat Sink	DNG1102
	25	Earth Plate	DNH2532
	26	Bottom Plate	See Contrast table(2)
	27	Bottom Earth Plate	DNH2694
	28	Trans Plate	DNH2733
NSP	29	Chassis	See Contrast table(2)
	30	Insulator Assembly	DXA2069
	31	Damper	CNV6011
	32	Earth Spring	DBH1398
	33	Float Spring (G5)	DBH1494
	34	Front Sheet	DED1132
	35	Mecha Plate	DNH2642
	36	PCB Holder	DNK4524
	37	Float Base 04 Assy	DXB1838
	38	Laser Caution	See Contrast table(2)
NSP	39	Serial Label (UPC)	See Contrast table(2)
	40	Screw	BBT30P060FCC
	41	Screw	BBZ30P060FTC
	42	Screw	BBZ30P100FTC
	43	Screw	BBZ40P060FTC
	44	Screw	BPZ30P080FTB
	45	DM Screw (FTC)	DBA1260
	46	Screw	IPZ30P100FTC

(2) CONTRAST TABLE

CDJ-800MK2/KUCXJ, /WYXJ5 and RLFXJ types are constructed the same except for the following:

Mark	No.	Symbol and Description	CDJ-800MK2/ KUCXJ	CDJ-800MK2/ WYXJ5	CDJ-800MK2/ RLFXJ
⚠	2	AC IN ASSY	DWR1430	DWR1429	DWR1432
⚠	3	TRANS ASSY	DWR1371	DWR1371	DWR1428
⚠	10	Fuse (T1.6A)	AEK7075	Not used	Not used
⚠	10	Fuse (800MA)	Not used	REK1021	REK1021
⚠	17	Power Transfomer	DTT1204	DTT1203	DTT1203
	26	Bottom Plate	DNK2689	DNK2689	DNK2691
	29	Chassis	DNK4518	DNK4517	DNK4519
	38	Laser Caution	DRW2308	DRW2308	DRW2248
NSP	39	Serial Label	DRW2311	VRW1629	VRW1629

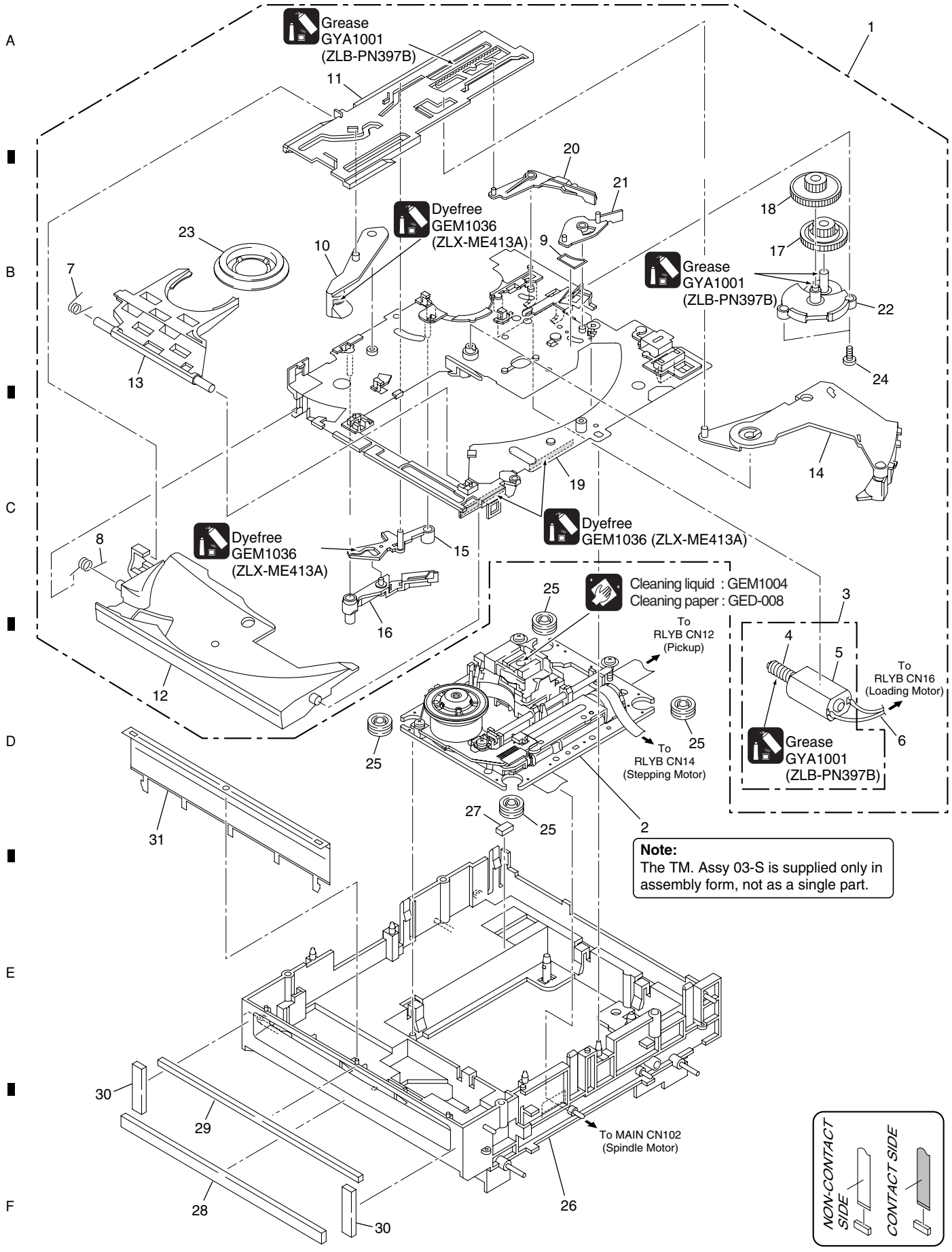
2.3 CONTROL PANEL SECTION



CONTROL PANEL SECTION parts List

Mark	No.	Description	Part No.
	1	DFLB Assy	DWG1623
	2	KSWB Assy	DWS1386
	3	JFLB Assy	DWG1624
	4	SLDB Assy	DWS1387
	5	JOGB Assy	DWG1625
	6	FFC	DDD1220
	7	Connector Assy	PF04PP-B07
	8	Jog Panel (PMMA)	DAH2182
	9	Jog Plate	DAH2438
	10	SW spring 25	DBH1514
	11	Gear spring 200	DBH1525
	12	ARM Sprimg	DBH1566
	13	SW Cushion HH48/2	DEC2538
	14	Encorder Plate	DEC2889
	15	Protector Sheet	DEC2945
	16	FL Sheet	DEC2946
	17	Ring Cushion L24/2.0	DEC2958
	18	SW Ring	DNK4070
	19	Adjust Plate	DNK4178
	20	Jog Holder	DNK4545
	21	Jog B	DNK4557
	22	Gear ARM	DNK4559
	23	Gear	DNK4560
	24	Smoother	DNK4561
	25	Load Gear A	DNK4562
	26	Jog A	DNK4586
	27	Sheet SW	DSX1065
	28	Roller A Assy	DXB1825
	29	Jog Stay Assy	DXB1876
	30	Roller B Assy	DXB1877
	31	Rotary Knob C	DAA1194
	32	TEMPO Knob	DAC2061
	33	VINYL Knob	DAC2063
	34	LOOP Knob	DAC2066
	35	Auto Beat Loop Knob	DAC2069
	36	Quick Return Knob	DAC2070
	37	PLAY Knob	DAC2286
	38	Set Knob (Eject)	DAC2287
	39	CALL Knob	DAC2289
	40	RELOOP Knob	DAC2291
	41	Slide Knob	DAC2292
	42	TEXT/A.CUE Knob	DAC2294
	43	Folder Search Knob	DAC2298
	44	DEL/MEMO Knob	DAC2299
	45	Reverse Knob	DAC2364
	46	Slide Sheet (gray)	DAH2374
	47	Display Panel	DAH2418
	48	Earth Plate (CU)	DBK1224
	49	Vessel Sheet	DEC2495
	50	FFC Guard	DEC2586
	51	Reloop Guard	DNK4057
	52	Q R Guard	DNK4058
	53	Control Panel	DNK4525
	54	Screw	BPZ20P060FTC
	55	Screw	BPZ20P100FTC
	56	Screw (FE)	DBA1265
	57	Screw	IPZ30P100FTC
	58	Screw	BPZ30P080FTB
	59	Ecsane Tape (10x50)	DEC2988
	60	Cord Clamper	RNH-184-0
	61	Washer	WA42D080D050

2.4 SLOT-IN MECHANISM SECTION



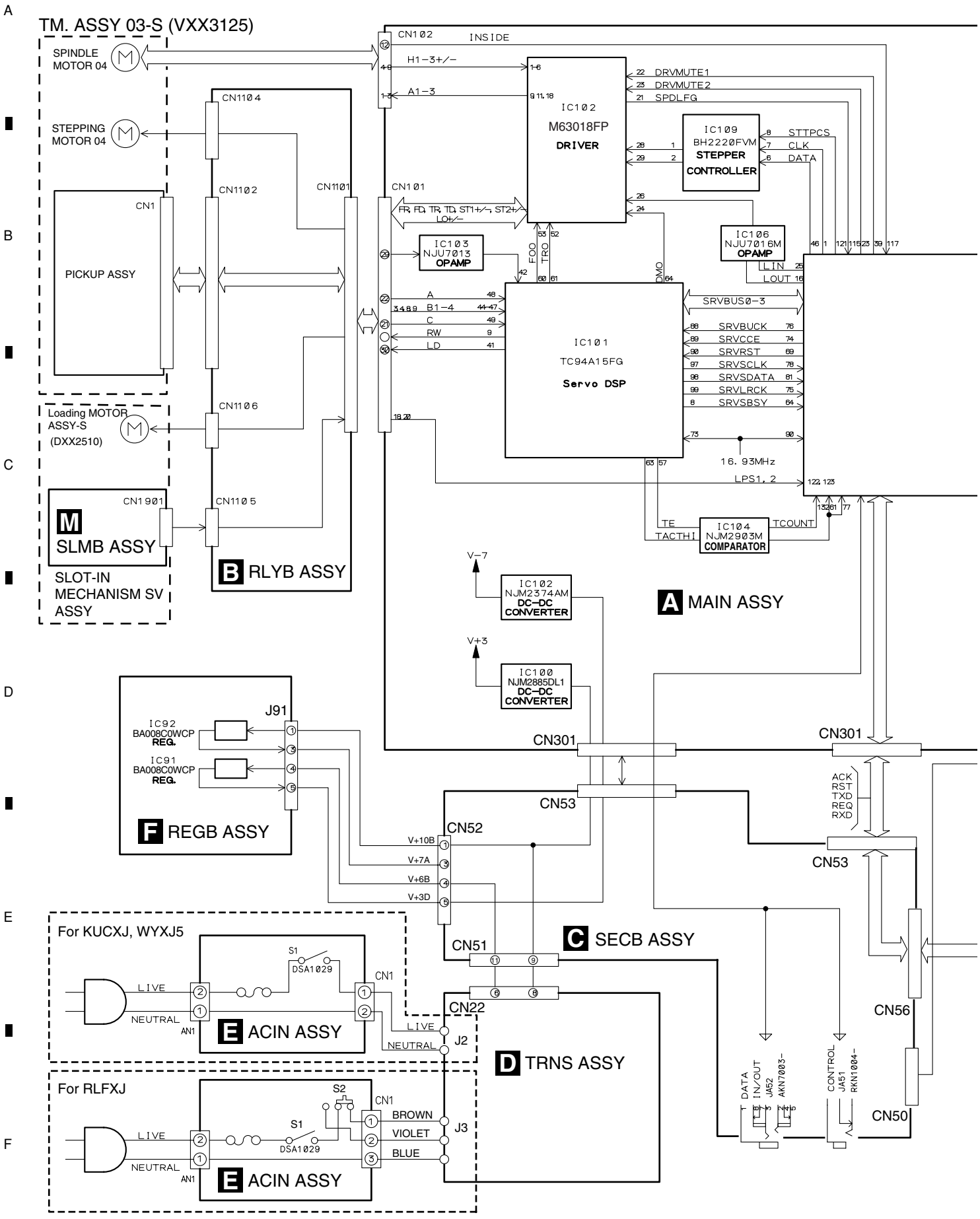
Note:
The TM. Assy 03-S is supplied only in assembly form, not as a single part.

SLOT-IN MECHANISM SECTION parts List

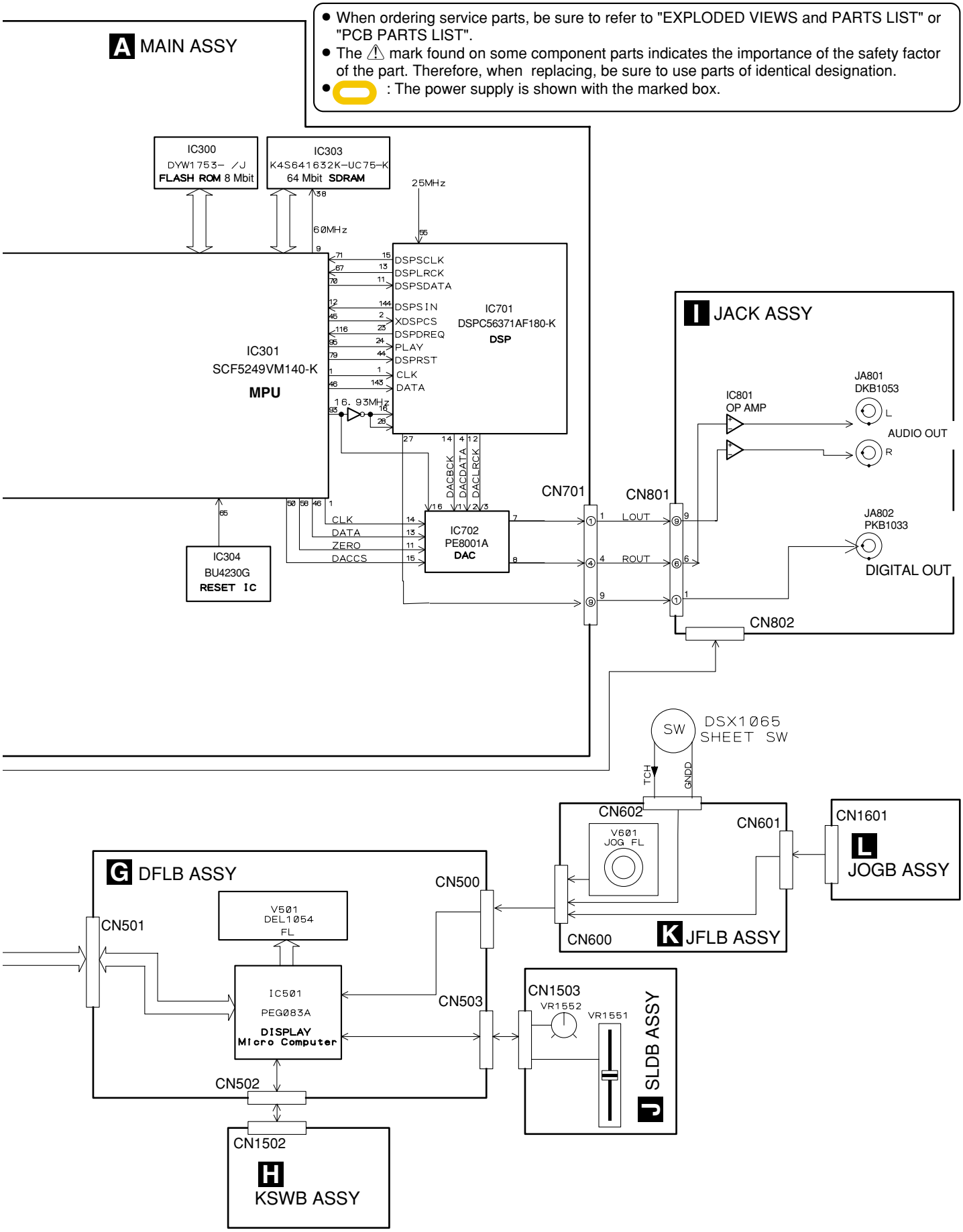
Mark	No.	Description	Part No.
NSP	1	Slot-in Mecha SV Assy	DXA2005
	2	TM. Assy 03-S	VXX3125
	3	Loading Motor Assy-S	DXX2510
NSP	4	Worm Gear	DNK3910
NSP	5	DC Motor S (ROHS)	DXM1230
	6	Connector Assy	PF02PY-B22
	7	Clamp Spring	DBH1374
	8	Guide Spring	DBH1375
	9	SW Lever Spacer SV	DEC2831
	10	Loading Lever	DNK3406
	11	Main Cam	DNK3407
	12	Disc Guide	DNK3478
	13	Clamp Arm	DNK3576
	14	Eject Lever	DNK3684
	15	Lever AP	DNK3835
	16	Lever BP	DNK3836
	17	Loading Gear	DNK3911
	18	Drive Gear	DNK3912
	19	Loading Base SV	DNK4369
	20	SW Lever SV1	DNK4370
	21	SW Lever SV2	DNK4371
	22	Gear Holder SV	DNK4372
	23	Clamper 04 Assy	DXB1859
	24	Screw	BPZ20P060FTC
	25	Floating Rubber (SI)	VEB1351
	26	Float Base 04 Assy	DXB1838
	27	Spacer POR (T3)	DEB1566
	28	Vessel Cushion A	DEC2852
	29	Vessel Cushion B	DEC2853
	30	Vessel Cushion C	DEC2854
	31	Front Sheet	DED1132

3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM

3.1 BLOCK DIAGRAM

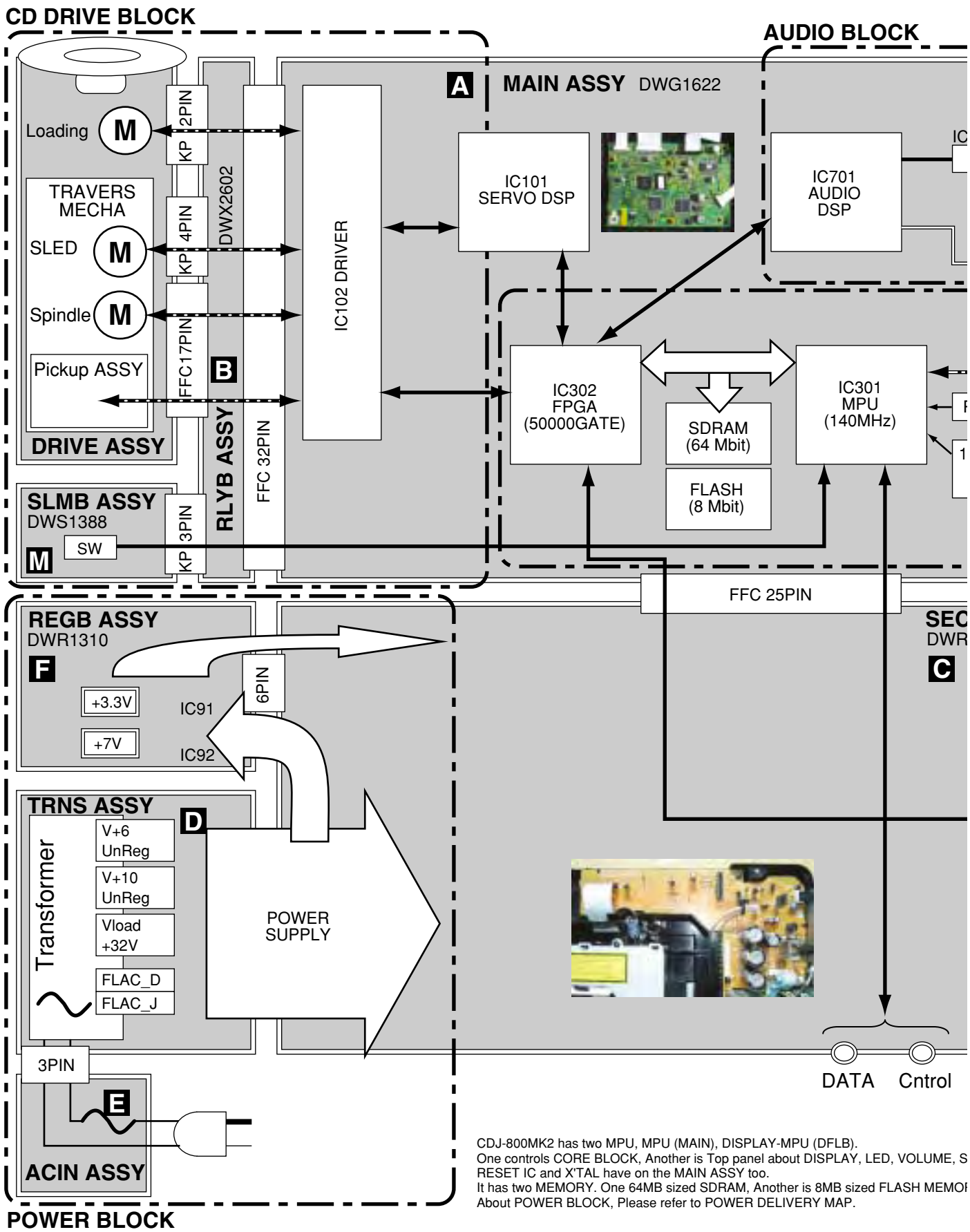


- When ordering service parts, be sure to refer to "EXPLODED VIEWS and PARTS LIST" or "PCB PARTS LIST".
- The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
- : The power supply is shown with the marked box.

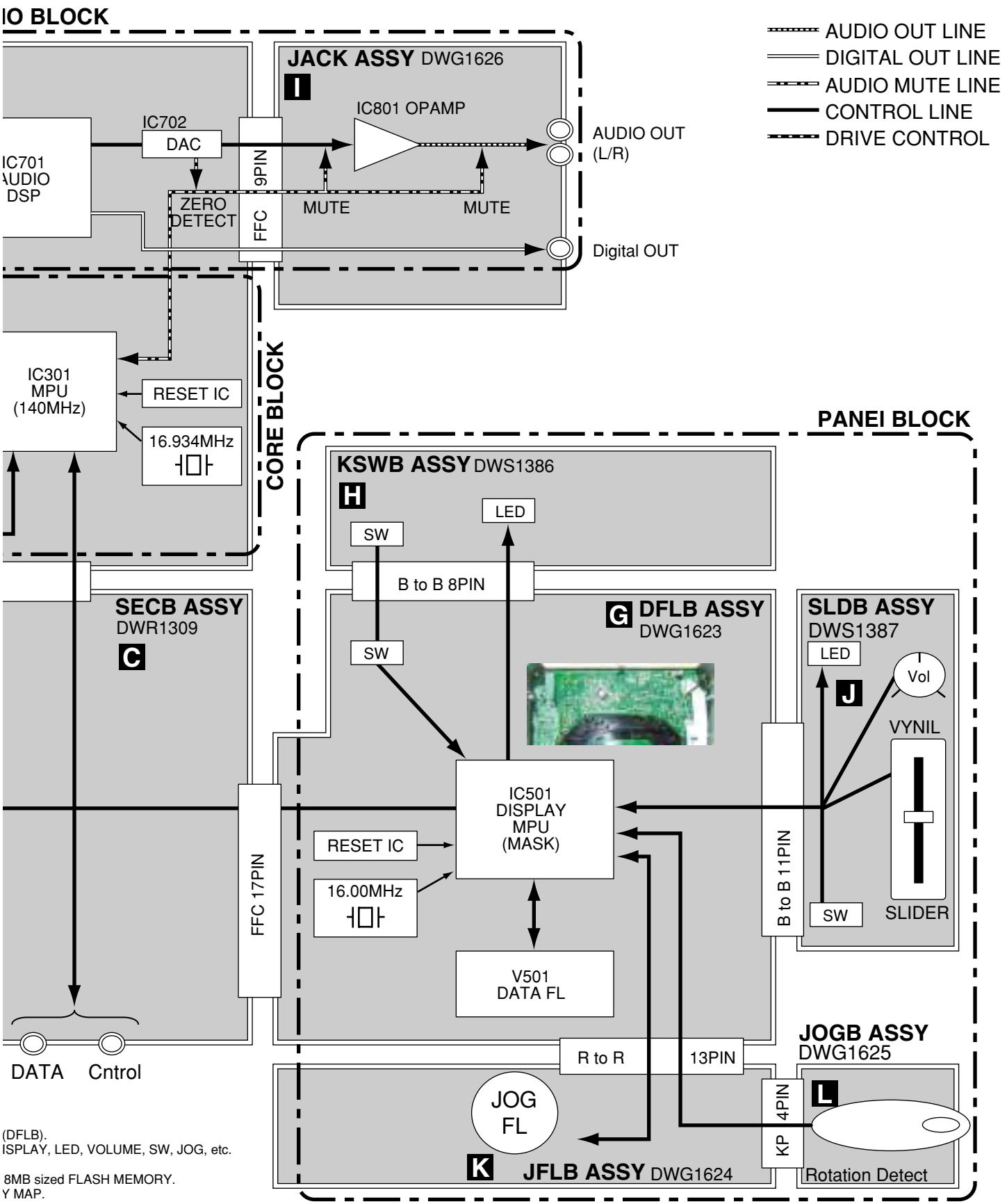


3.2 BLOCK DIAGRAM (2)

• Blick diagra Map

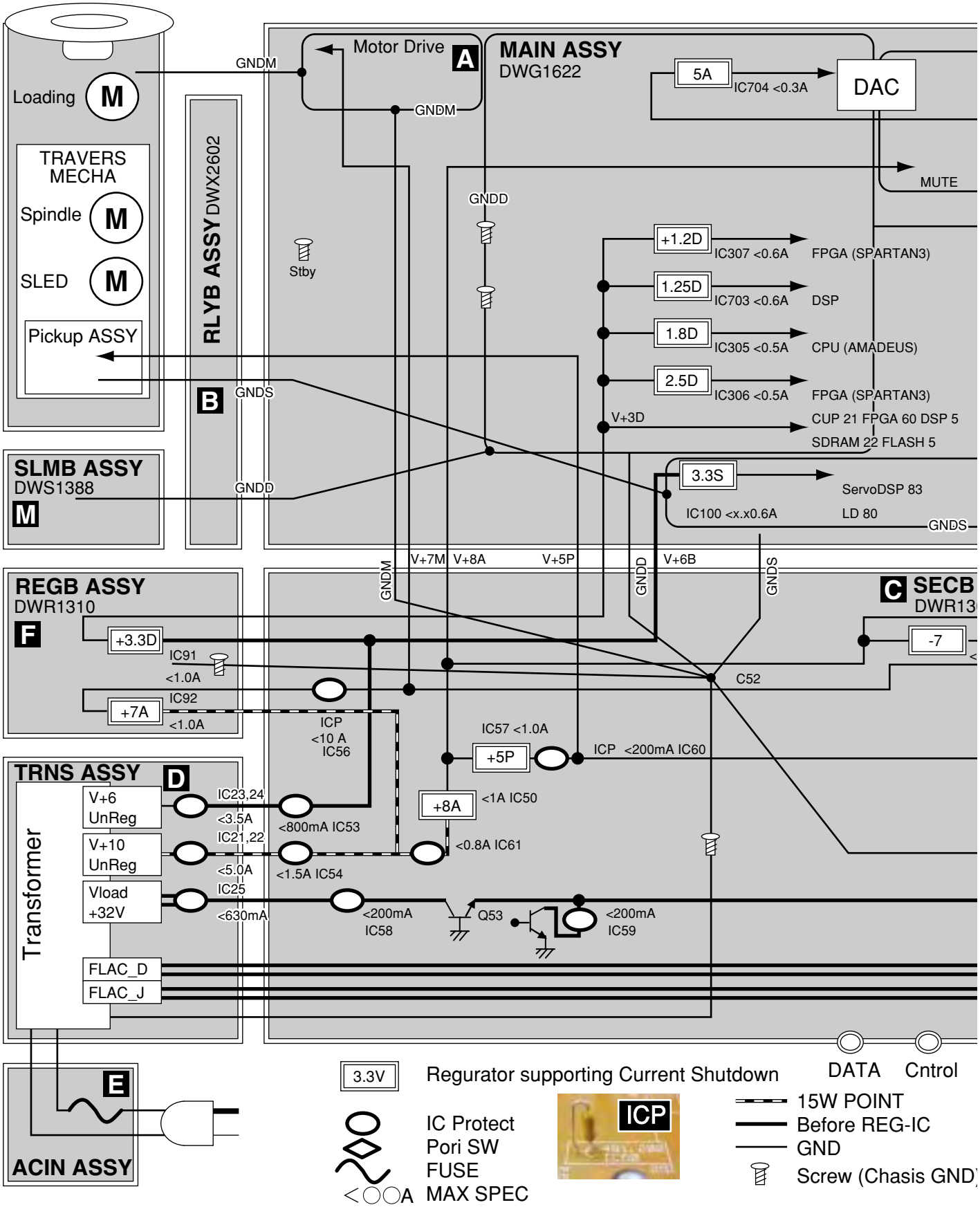


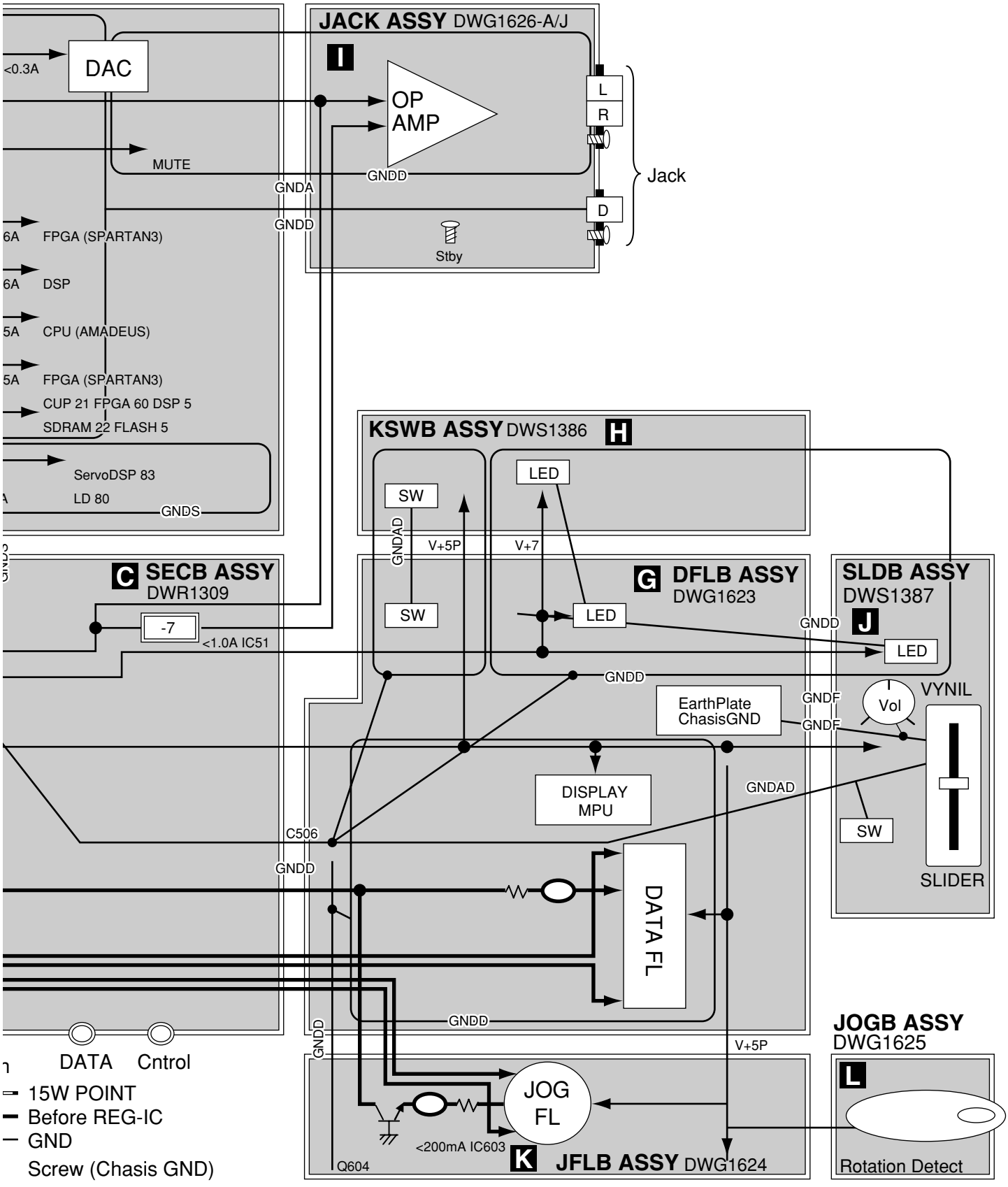
CDJ-800MK2 has two MPU, MPU (MAIN), DISPLAY-MPU (DFLB).
One controls CORE BLOCK, Another is Top panel about DISPLAY, LED, VOLUME, S
RESET IC and X'TAL have on the MAIN ASSY too.
It has two MEMORY. One 64MB sized SDRAM, Another is 8MB sized FLASH MEMOI
About POWER BLOCK, Please refer to POWER DELIVERY MAP.


IO BLOCK
AUDIO OUT LINE
DIGITAL OUT LINE
AUDIO MUTE LINE
CONTROL LINE
DRIVE CONTROL
JACK ASSY DWG1626
I
IC801 OPAMP
IC702
DAC
IC701
AUDIO
DSP
9PIN
FFC
ZERO
DETECT
MUTE
MUTE
AUDIO OUT
(L/R)
Digital OUT
IC301
MPU
(140MHz)
RESET IC
16.934MHz
CORE BLOCK
PANEI BLOCK
KSWB ASSY DWS1386
H
LED
SW
B to B 8PIN
SECB ASSY
DWR1309
C
G DFLB ASSY
DWG1623
SW
SLDB ASSY
DWS1387
LED
J
Vol
VYNIL
IC501
DISPLAY
MPU
(MASK)
RESET IC
16.00MHz
FFC 17PIN
B to B 11PIN
SW
SLIDER
V501
DATA FL
DATA
Cntrol
R to R
13PIN
JOGB ASSY
DWG1625
JOG
FL
4PIN
KP
L
K
JFLB ASSY DWG1624
Rotation Detect
(DFLB).
ISPLAY, LED, VOLUME, SW, JOG, etc.
8MB sized FLASH MEMORY.
Y MAP.

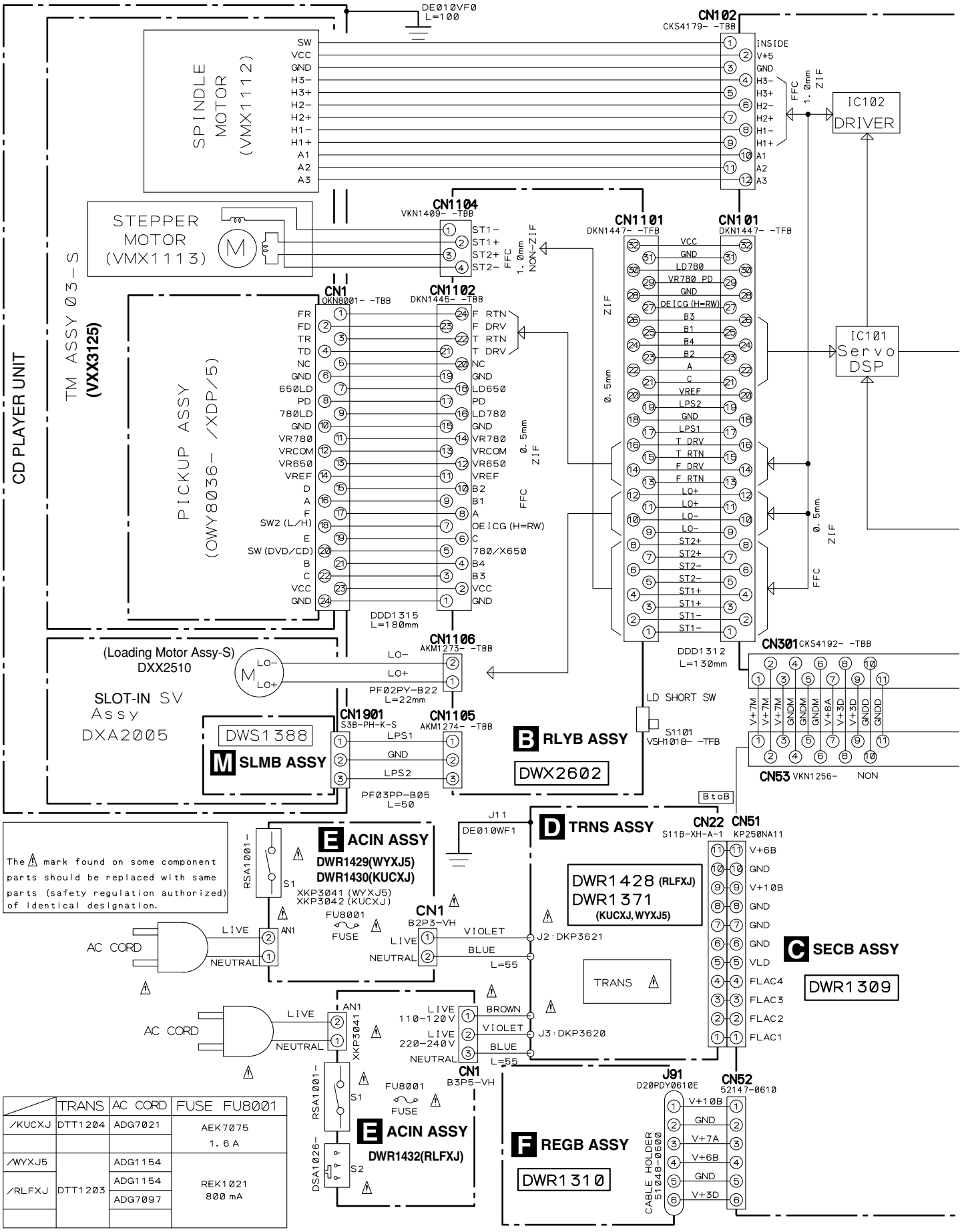
3.3 BLOCK DIAGRAM (Power)

• Power Delivery Map

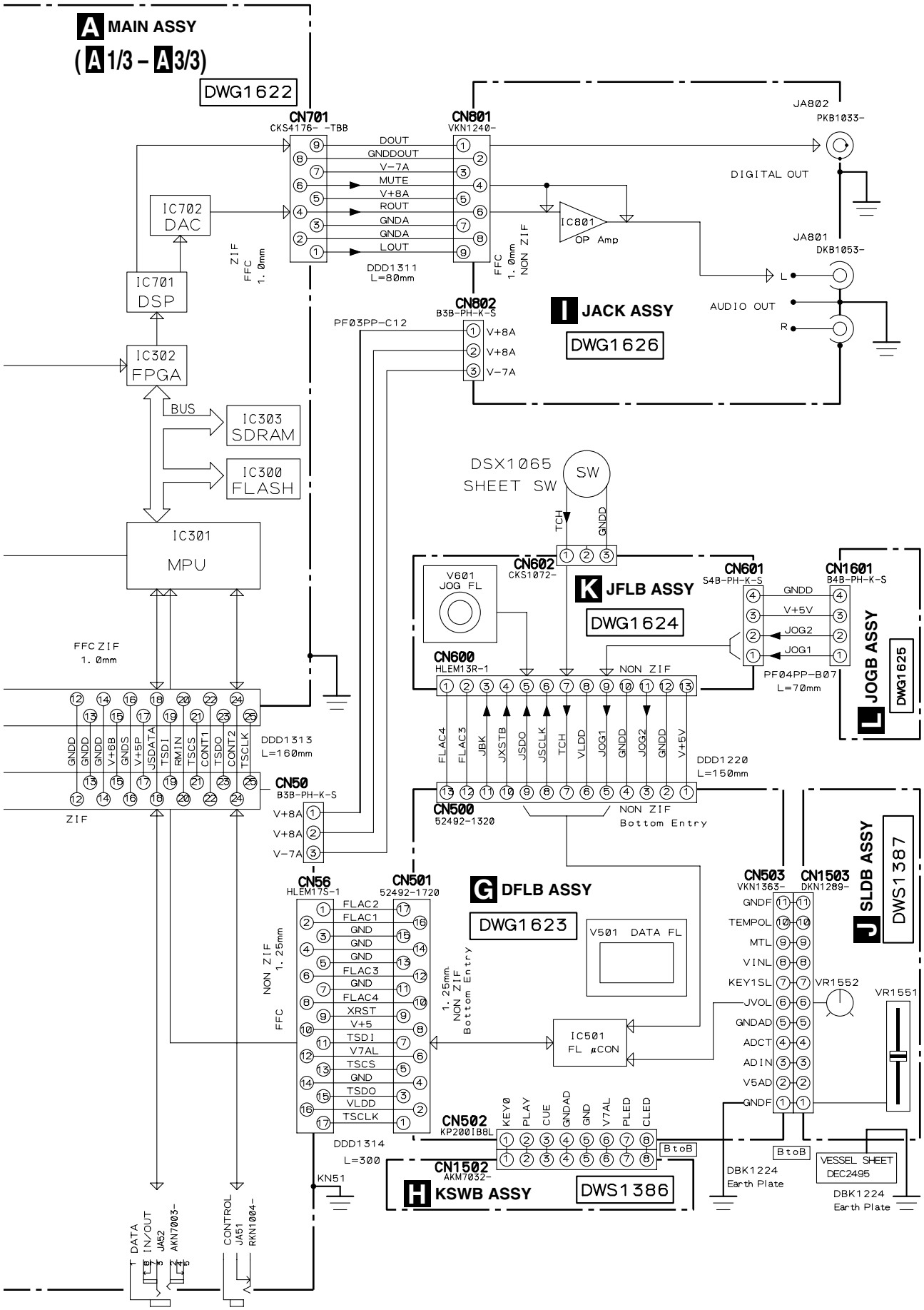



JACK ASSY DWG1626-A/J
I
DAC
<0.3A
OP AMP
MUTE
GNDD
GNDA
GNDD
L
R
D
Jack
Stby
6A FPGA (SPARTAN3)
6A DSP
5A CPU (AMADEUS)
5A FPGA (SPARTAN3)
CUP 21 FPGA 60 DSP 5
SDRAM 22 FLASH 5
ServoDSP 83
LD 80
GNDS
KSWB ASSY DWS1386
H
LED
SW
GNDAD
V+5P
V+7
C SECB ASSY
DWR1309
-7
<1.0A IC51
G DFLB ASSY
DWG1623
SW
LED
SLDB ASSY
DWS1387
J
GNDD
LED
GNDD
EarthPlate
ChasisGND
GNDF
GNDF
Vol
VYNIL
DISPLAY
MPU
GNDAD
SW
SLIDER
C506
GNDD
DATA FL
GNDD
GNDD
V+5P
JOGB ASSY
DWG1625
L
JOG
FL
<200mA IC603
K JFLB ASSY DWG1624
Q604
Rotation Detect
DATA
Cntrol
15W POINT
Before REG-IC
GND
Screw (Chasis GND)

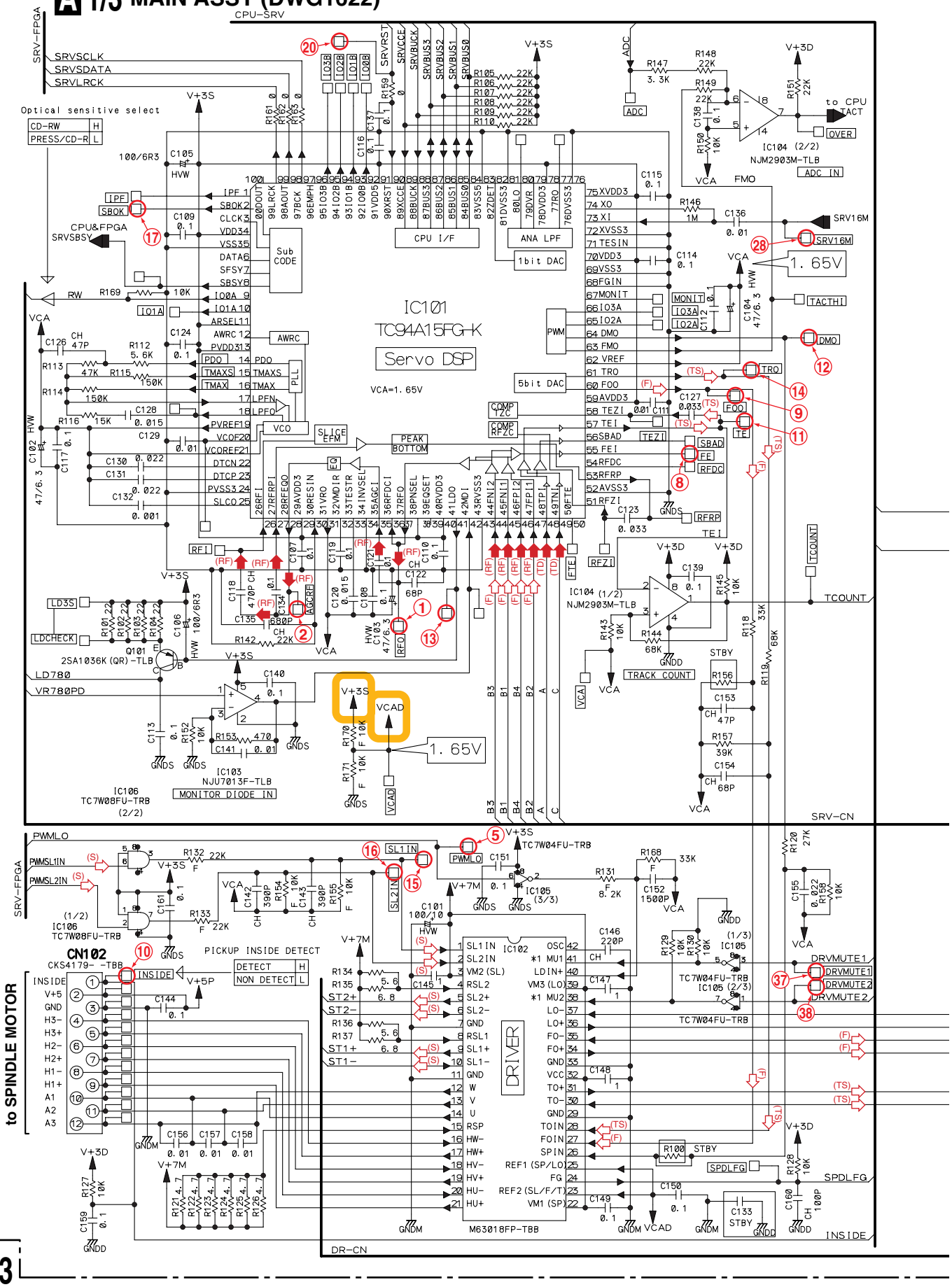
3.4 OVERALL WIRING DIAGRAM

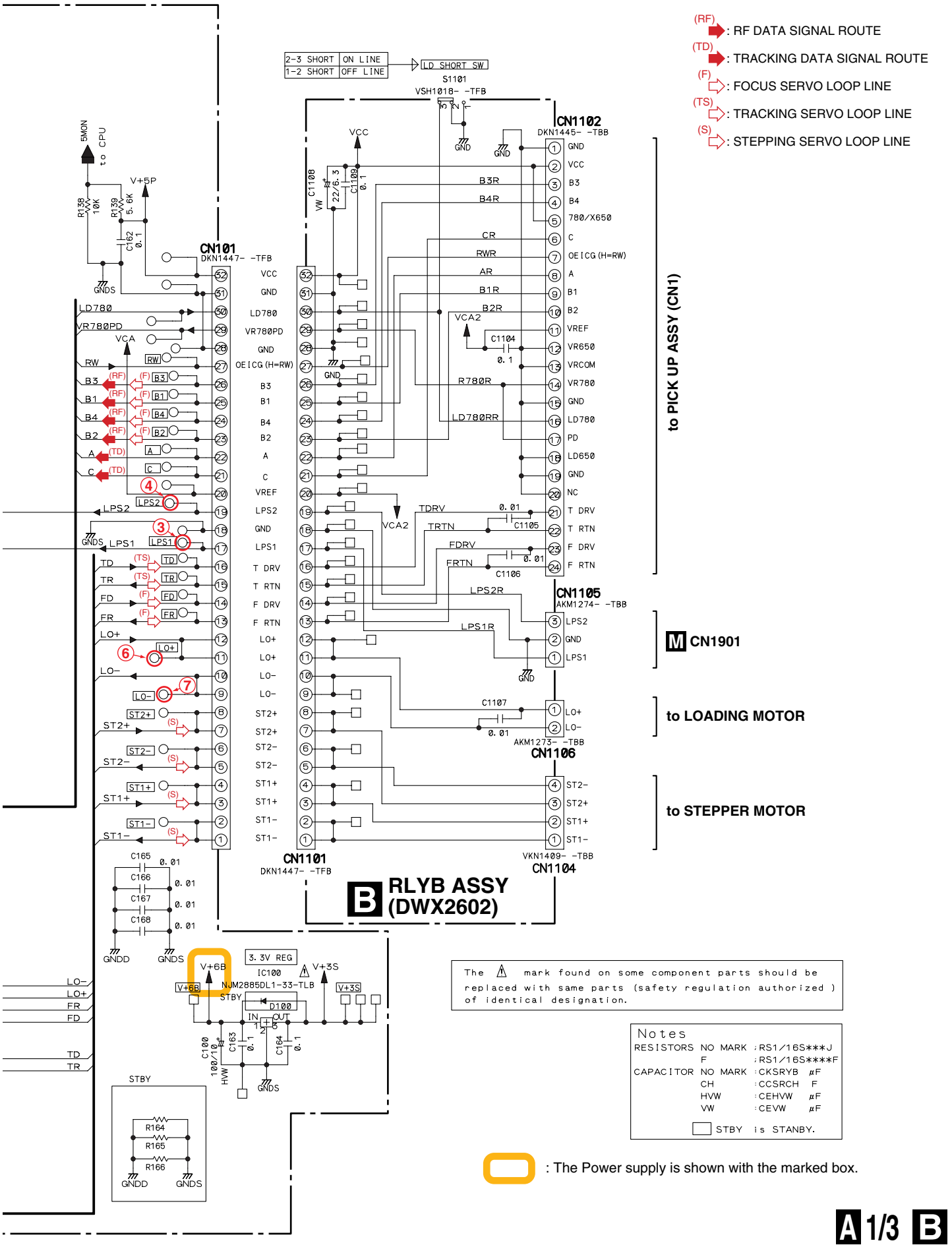


	TRANS	AC CORD	FUSE FU8001
/KUCXJ	DTT1204	ADG7021	AEK7075 1.6A
/WYXJ5	DTT1203	ADG1154	REK1021 800mA
/RLFXJ		ADG1154	
		ADG7097	


A MAIN ASSY
(A 1/3 – A 3/3)
DWG1622
CN701
CKS4176- -TBB
CN801
VKN1240-
DOUT
GNDDOUT
V-7A
MUTE
V+8A
ROUT
GNDA
GNDA
LOUT
DDD1311
L=80mm
FFC
1.0mm
NON ZIF
IC702
DAC
IC701
DSP
IC302
FPGA
BUS
IC303
SDRAM
IC300
FLASH
IC301
MPU
IC801
OP Amp
JA802
PKB1033-
DIGITAL OUT
JA801
DKB1053-
L
AUDIO OUT
R
CN802
B3B-PH-K-S
PF03PP-C12
V+8A
V+8A
V-7A
I JACK ASSY
DWG1626
DSX1065
SHEET SW
SW
TCH
GNDD
CN602
CKS1072-
V601
JOG FL
K JFLB ASSY
DWG1624
CN601
S4B-PH-K-S
CN1601
B4B-PH-K-S
GNDD
V+5V
JOG2
JOG1
PF04PP-B07
L=70mm
L JOGB ASSY
DWG1625
CN600
HLEM13R-1
NON ZIF
FFC ZIF
1.0mm
GNDD
GNDD
GNDD
V+6B
GNDS
V+5P
JSDATA
TSDI
RMIN
TSCS
CONT1
TSDO
CONT2
TSCLK
DDD1313
L=160mm
ZIF
CN50
B3B-PH-K-S
V+8A
V+8A
V-7A
FLAC4
FLAC3
JBK
JXSTB
JSDO
JSCLK
TCH
VLDD
JOG1
GNDD
JOG2
GNDD
V+5V
DDD1220
L=150mm
CN500
52492-1320
NON ZIF
Bottom Entry
CN56
HLEM17S-1
CN501
52492-1720
G DFLB ASSY
DWG1623
V501 DATA FL
FLAC2
FLAC1
GND
GND
GND
FLAC3
GND
FLAC4
XRST
V+5
TSDI
V7AL
TSCS
GND
TSDO
VLDD
TSCLK
NON ZIF
1.25mm
FFC
1.25mm
NON ZIF
Bottom Entry
IC501
FL μCON
CN503
VKN1363-
CN1503
DKN1289-
J SLDB ASSY
DWS1387
GNDF
TEMPOL
MTL
VINL
KEY1SL
JVOL
GNDAD
ADCT
ADIN
V5AD
GNDF
VR1552
VR1551
CN502
KP200IB8L
KEY0
PLAY
CUE
GNDAD
GND
V7AL
PLED
CLED
BtoB
BtoB
DDD1314
L=300
CN1502
AKM7032-
H KSWB ASSY
DWS1386
KN51
DBK1224
Earth Plate
VESSEL SHEET
DEC2495
DBK1224
Earth Plate
DATA
IN/OUT
JA52
AKN7003-
CONTROL
JA51
RKN1004-

A 1/3 MAIN ASSY (DWG1622)

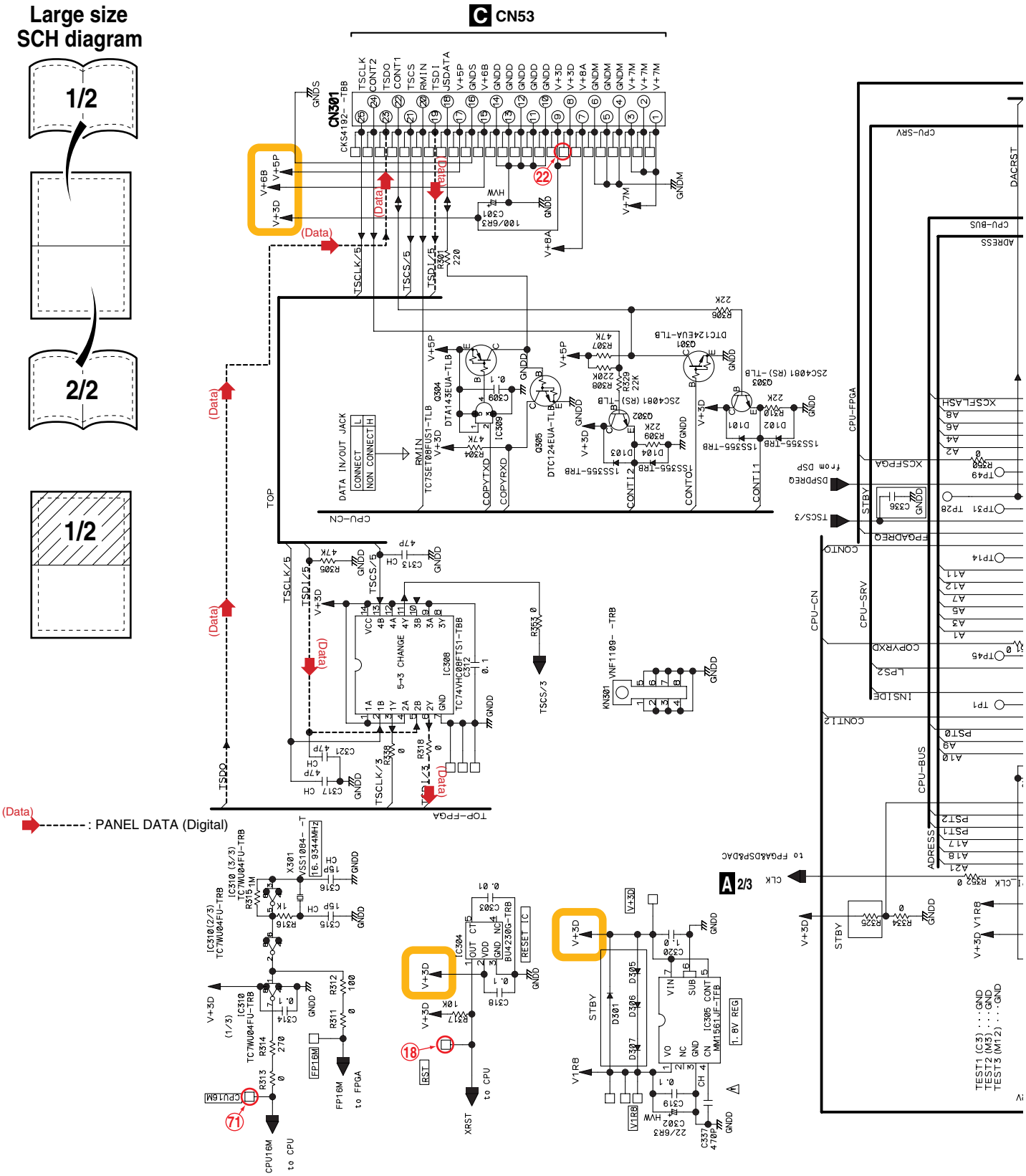



(RF) : RF DATA SIGNAL ROUTE
(TD) : TRACKING DATA SIGNAL ROUTE
(F) : FOCUS SERVO LOOP LINE
(TS) : TRACKING SERVO LOOP LINE
(S) : STEPPING SERVO LOOP LINE
2-3 SHORT ON LINE
1-2 SHORT OFF LINE
LD SHORT SW
S1101
VSH1018- -TFB
CN1102
DKN1445- -TBB
CN101
DKN1447- -TFB
CN1105
AKM1274- -TBB
CN1106
AKM1273- -TBB
CN1101
DKN1447- -TFB
CN1104
VKN1409- -TBB
to PICK UP ASSY (CN1)
M CN1901
to LOADING MOTOR
to STEPPER MOTOR
B RLYB ASSY (DWX2602)
5MON
to CPU
V+5P
GNDS
VCC
GND
LD780
VR780PD
VCA
RW
OEICG (H=RW)
B3
B1
B4
B2
A
C
VREF
LPS2
LPS1
T DRV
T RTN
F DRV
F RTN
LO+
LO−
ST2+
ST2−
ST1+
ST1−
B3R
B4R
780/X650
CR
RWR
AR
B1R
B2R
VCA2
VR650
VRCOM
VR780
R780R
LD780RR
PD
LD650
NC
TDRV
TRTN
FDRV
FRTN
LPS2R
LPS1R
C1104
C1105
C1106
C1107
C1108
C1109
GNDD
3.3V REG
IC100
NJM2885DL1-33-TLB
V+6B
V+3S
STBY
D100
IN
OUT
C100
C163
C164
HVW
R164
R165
R166
The ⚠ mark found on some component parts should be replaced with same parts (safety regulation authorized) of identical designation.
Notes
RESISTORS NO MARK ;RS1/16S***J
F ;RS1/16S****F
CAPACITOR NO MARK :CKSRYB μF
CH :CCSRCH F
HVW :CEHVW μF
VW :CEVW μF
STBY is STANBY.
: The Power supply is shown with the marked box.

3.6 MAIN ASSY(2/3)

A 2/3 MAIN ASSY (DWG1622) (1/2)

Large size SCH diagram



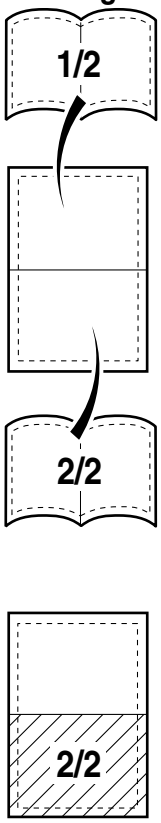
A 3/3
IC301
SCF5249VM140-K
CPU
from RESET IC
XRST
SRVSBSY
from SRV
V+3D
ZERO
XOE
to FPGA & FLASH
DATA
TACT
from SRV
LPS1
LPS2
R348 22K
R349 22K
R341 22K
CPU-DSP-DAC
CPU-SRV
CPU-BUS
CPU-CN
CPU-FPGA
ADRESS
DATA
DACRST
XFRST
XINIT
XDSPCS
FPGALRCK
DONE
ADC
SPDLFG
XWESDRAM
XCSSDRAM
SRVBUCK
SRVRST
DSPRST
FPGASCLK
SRVCCE
RX/XBY
TA
XCSFLASH
SDATA02/GPO41
LRCK2/GPIO44
SCL2/GPIO3
EBUOUT2/GPO37
EBUIN3/ADIN0/GPI38
EBUOUT1/GPO36
EBUIN2/GPI37
SDRAM_CS2/GPIO7
QSPI_DOUT/GPIO26
SDATA14/GPI42
LRCK4/GPIO46
SDA2/GPIO65
SDATA1_BS1/GPIO9
TOUT1/ADOUT/GPO35
SCLK2/GPIO48
EBUOUT1/GPO36
QSPI_CS0/GPIO29
SDRAM_CS1
TEST3
TEST2
TEST1
TEST0
RMIN
DACCS
MUTE
PRGM
FPGASBSY
FPGASDATA
SRVBUS0
SRVBUS1
CPU16M
SMON
from SRV
from 16M X'tal
TCOUNT
COPYTXD
LPS1
DSO
DSI
PSTCLK
PST3
BCLKE
DRVMUTE1
DRVMUTE2
STBY
BKPT
UDQM
SRVBUS2
DSCLK
CONTI1
SRVBUS3
DSPS_IN
PLAY
TEST1 (C3) : GND
TEST2 (M3) : GND
TEST3 (M12) : GND
TEST0 (C12) DSCLK (F11) TCK (E12)
DEBUG MODE PULL UP PULL UP OPEN
JTAG MODE GND GND GND

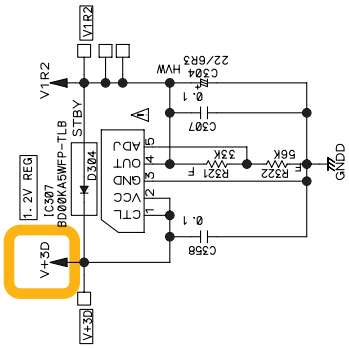
Notes
RESISTORS NO MARK :RS1/16S***J
F :RS1/16S****F
SS :RS1/16SS***J
CAPACITOR NO MARK :CKSRYB μF
CH :CCSRCH F
HVW :CEHVW μF
STBY is STANBY.

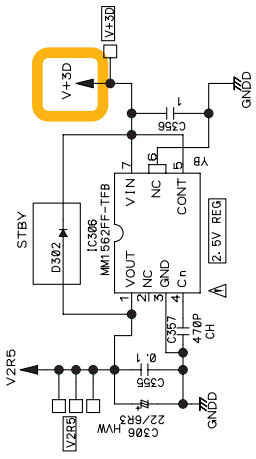
: The Power supply is shown with the marked box.

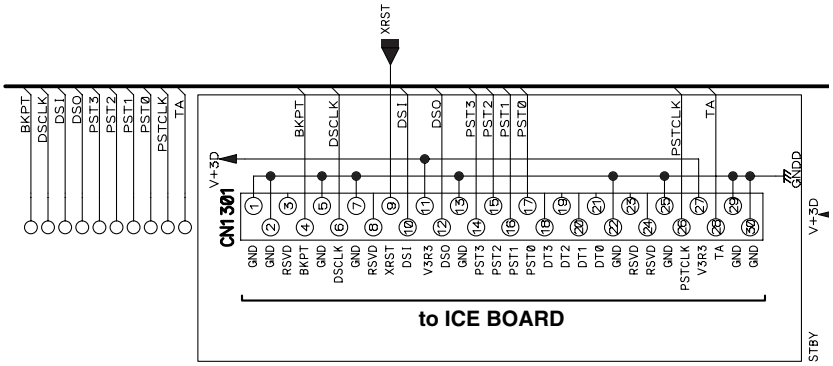
The mark found on some component parts should be replaced with same parts (safety regulation authorized) of identical designation.

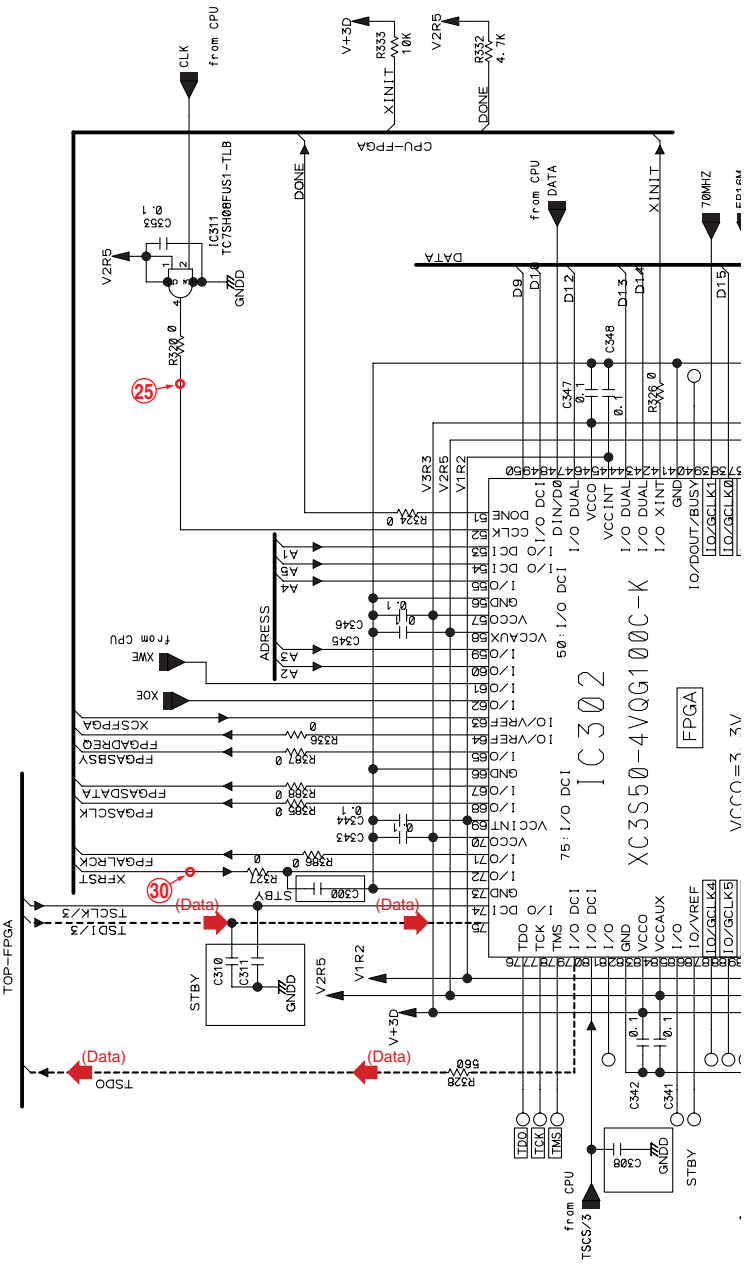
Large size SCH diagram

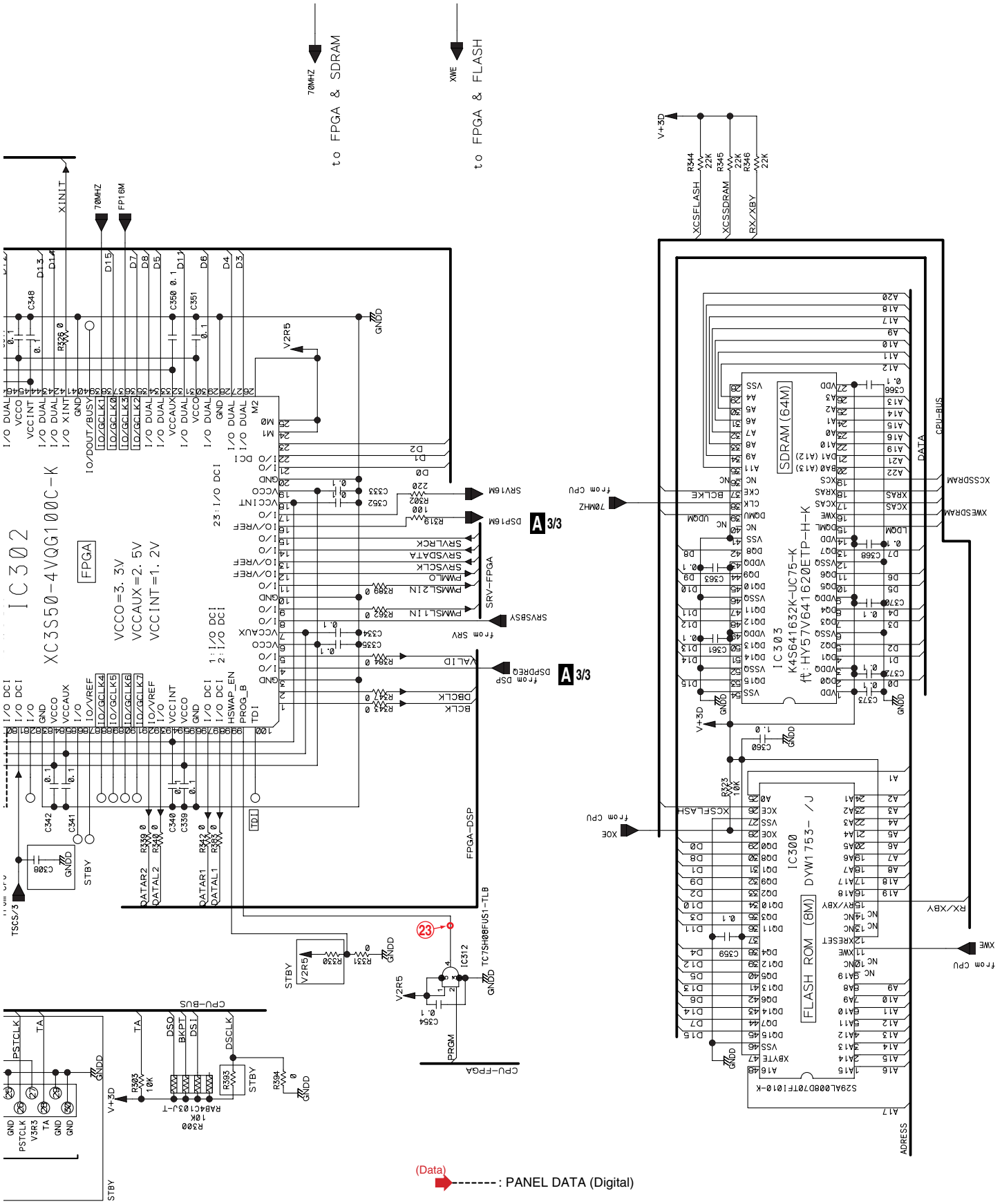




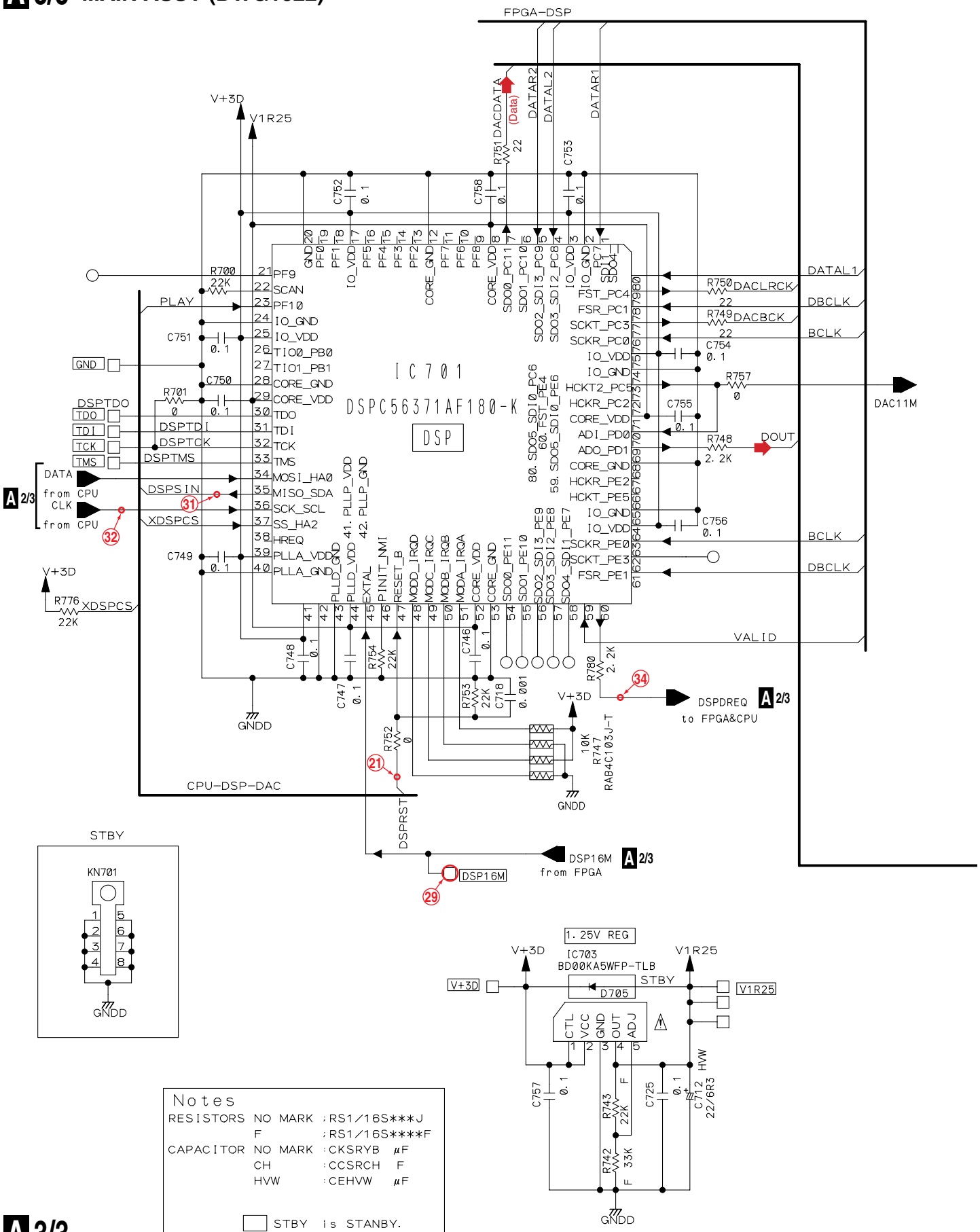


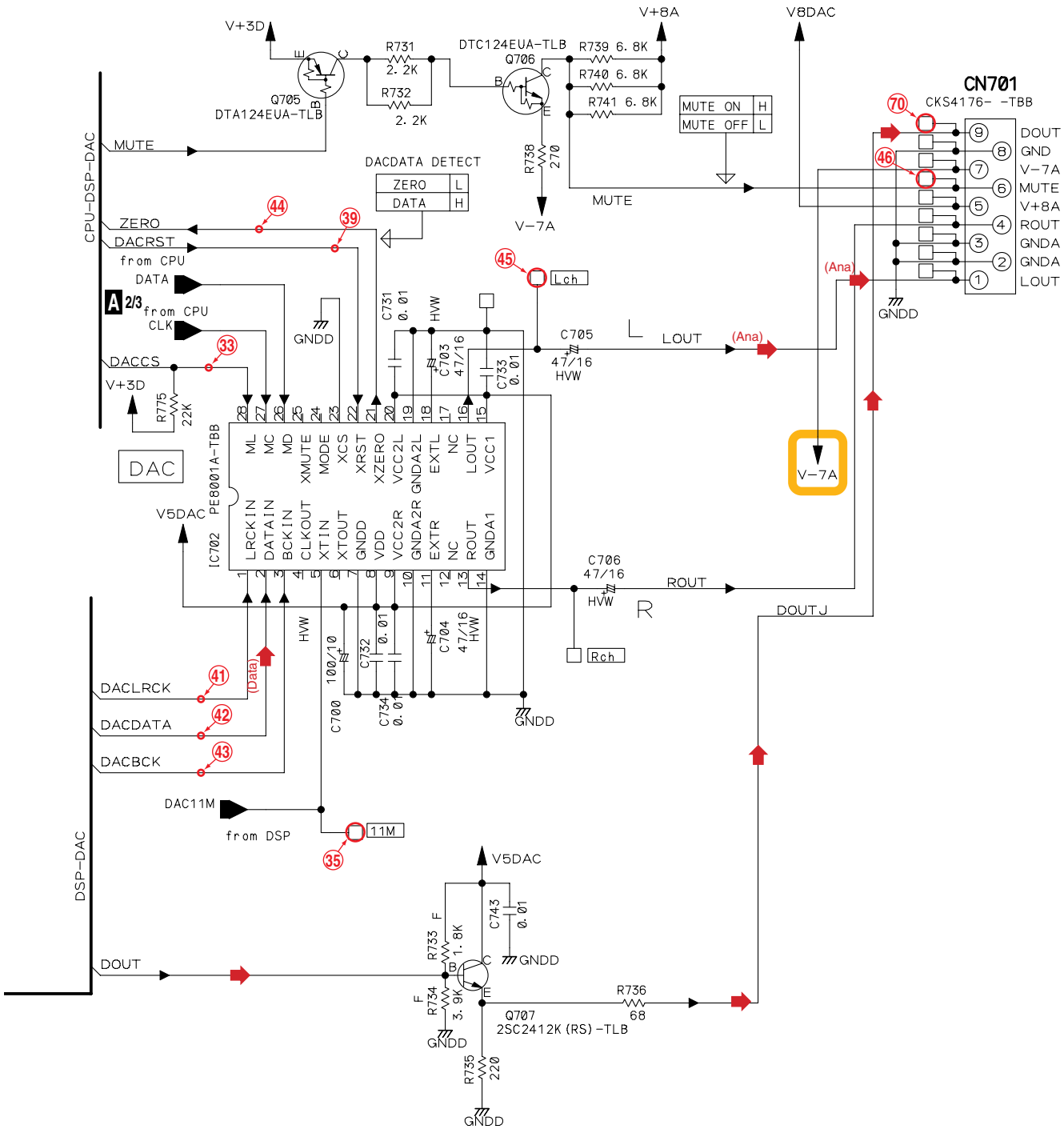




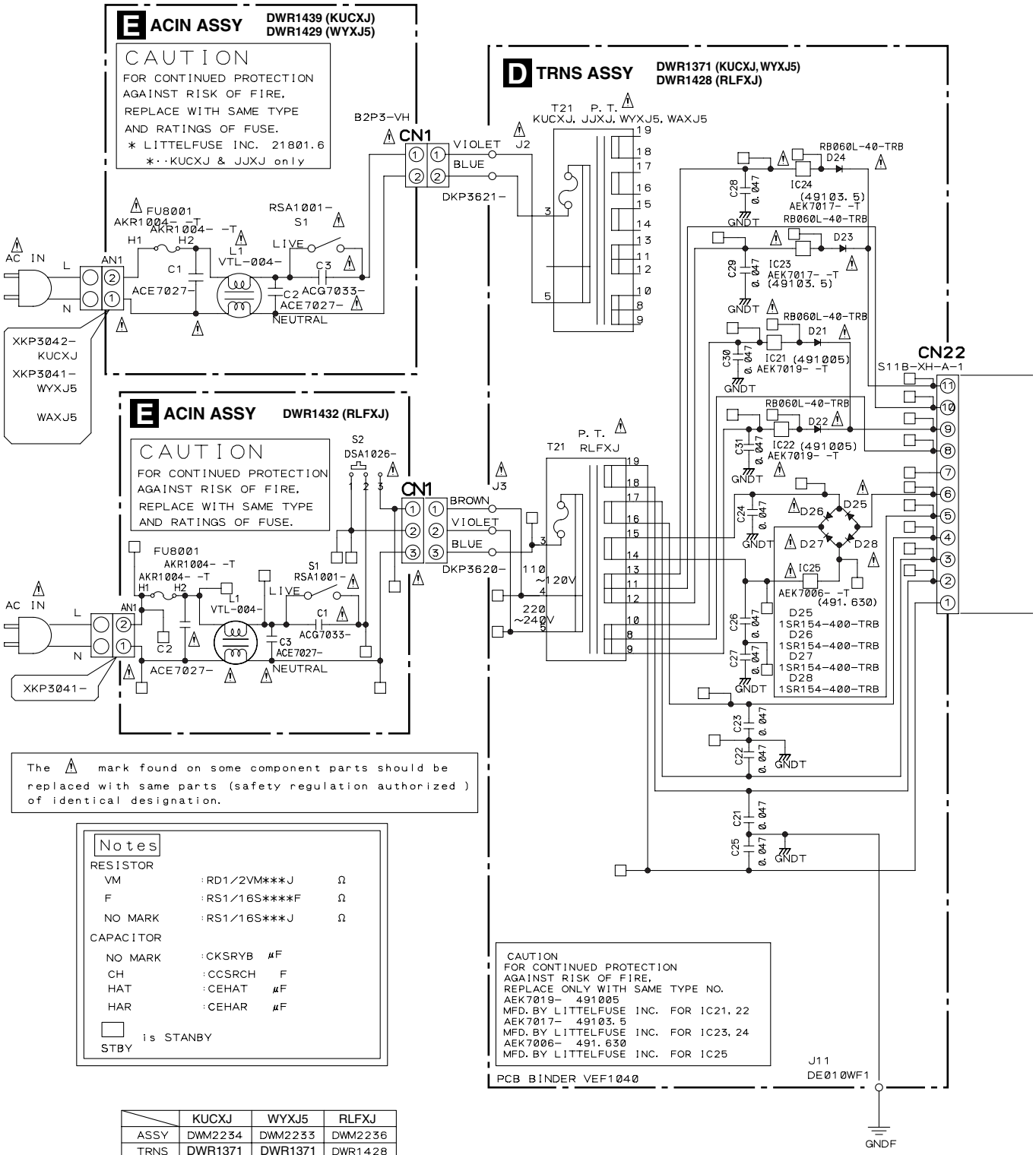

to FPGA & SDRAM
70MHZ
to FPGA & FLASH
XWE
IC302
XC3S50-4VQG100C-K
FPGA
VCCO=3. 3V
VCCAUX=2. 5V
VCCINT=1. 2V
XINIT
70MHZ
FP16M
V2R5
GNDD
SRV16M
DSP16M
A 3/3
SRV-FPGA
SRVSBSY
from SRV
DSPREQ
from DSP
DBCLK
TDI
STBY
FPGA-DSP
TSCS/3
IC312
TC7SH08FU(S1-TLB
CPU-FPGA
PRGM
CPU-BUS
PSTCLK
TA
DSO
BKPT
DSI
DSCLK
R303 10K
RAB4C103J-T
R300 10K
R393
R394 0
V+3D
XCSFLASH
XCSSDRAM
RX/XBY
R344 22K
R345 22K
R346 22K
SDRAM (64M)
IC303
K4S641632K-UC75-K
(1): HY57V641620ETP-H-K
DATA
CPU-BUS
XCSSDRAM
XWESDRAM
LDQM
UDQM
70MHZ
from CPU
XOE
IC300
DYW1753- /J
FLASH ROM (8M)
S29AL008D70TF1010-K
ADRESS
XWE
RX/XBY
(Data)
: PANEL DATA (Digital)

A 3/3 MAIN ASSY (DWG1622)

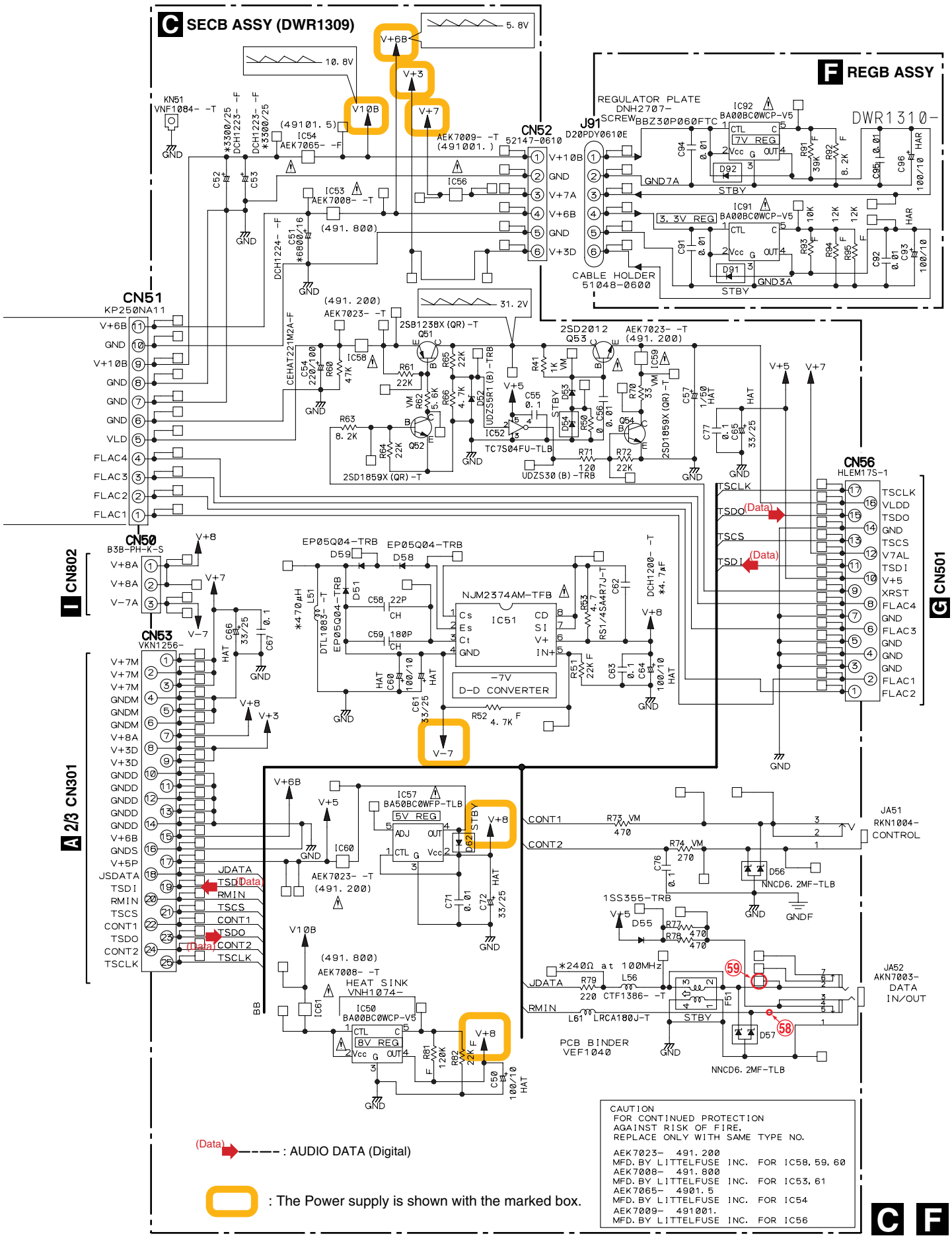


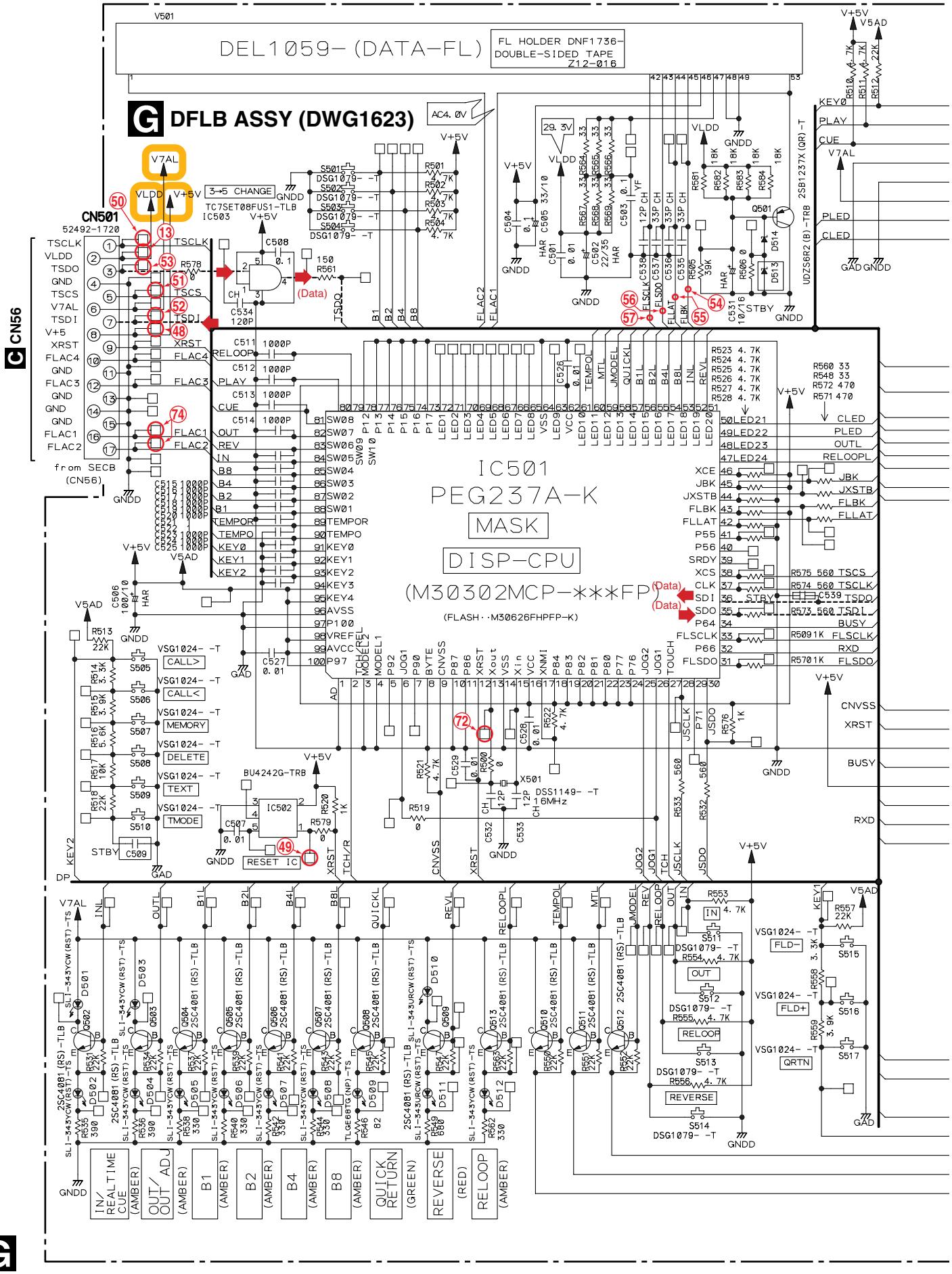

V+3D
V+8A
V8DAC
Q705
DTA124EUA-TLB
R731
2.2K
R732
2.2K
DTC124EUA-TLB
Q706
R739 6.8K
R740 6.8K
R741 6.8K
MUTE ON H
MUTE OFF L
CN701
CKS4176- -TBB
DOUT
GND
V-7A
MUTE
V+8A
ROUT
GNDA
GNDA
LOUT
CPU-DSP-DAC
MUTE
DACDATA DETECT
ZERO L
DATA H
R738
270
V-7A
ZERO
DACRST
from CPU
DATA
from CPU
CLK
DACCS
V+3D
R775
22K
GNDD
C731
0.01
HVW
C703
47/16
C733
0.01
Lch
C705
47/16
HVW
LOUT
(Ana)
DAC
IC702 PE8001A-TBB
ML MC MD XMUTE MODE XCS XRST XZERO VCC2L GNDA2L EXTL NC LOUT VCC1
LRCKIN DATAIN BCKIN CLKOUT XTIN XTOUT GNDD VDD VCC2R GNDA2R EXTR NC ROUT GNDA1
V5DAC
C706
47/16
HVW
ROUT
R
Rch
DOUTJ
C732
0.01
C704
47/16
HVW
C700
100/10
C734
0.01
GNDD
DACLRCK
DACDATA
DACBCK
(Data)
DAC11M
from DSP
11M
DSP-DAC
V5DAC
C743
0.01
R733
1.8K
GNDD
DOUT
R734
3.9K
GNDD
Q707
2SC2412K (RS) -TLB
R736
68
R735
220
GNDD
V8DAC
V+8A
C728
0.1
NJM2880U1-05-TLB
IC704
VIN
VOUT
STBY
D707
5V REG
C701
47/16
HVW
C729
0.1
GNDD
V5DAC
C702
100/10
HVW
C730
0.1
GNDD
The ⚠ mark found on some component parts should be replaced with same parts (safety regulation authorized) of identical designation.
: The Power supply is shown with the marked box.
(Data) : AUDIO DATA (Digital)
(Ana) : AUDIO Lch OUT (Analog)
: DATA AUDIO OUT (Digital)

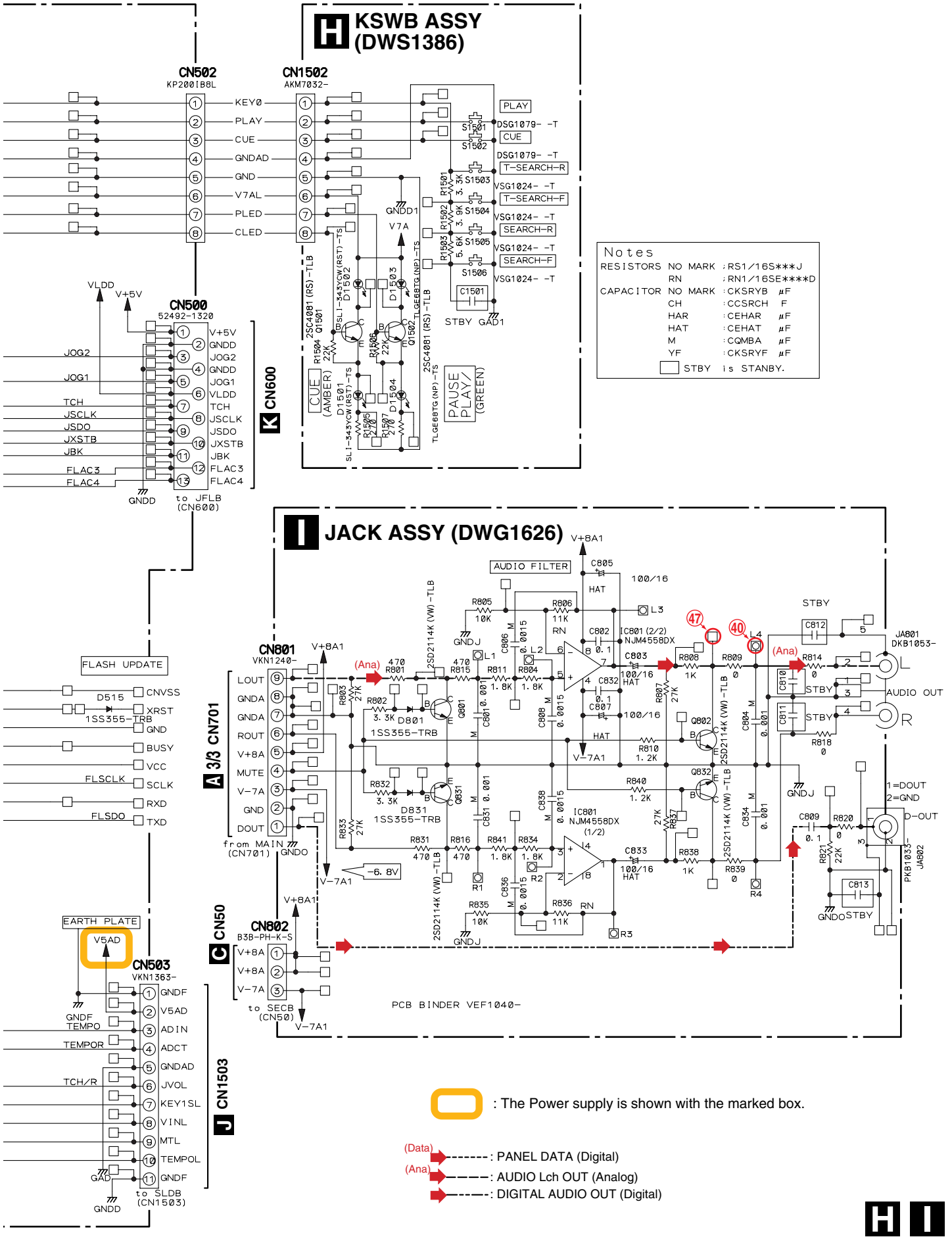
3.8 AC IN, TRNS, SECB and REGB ASSYS



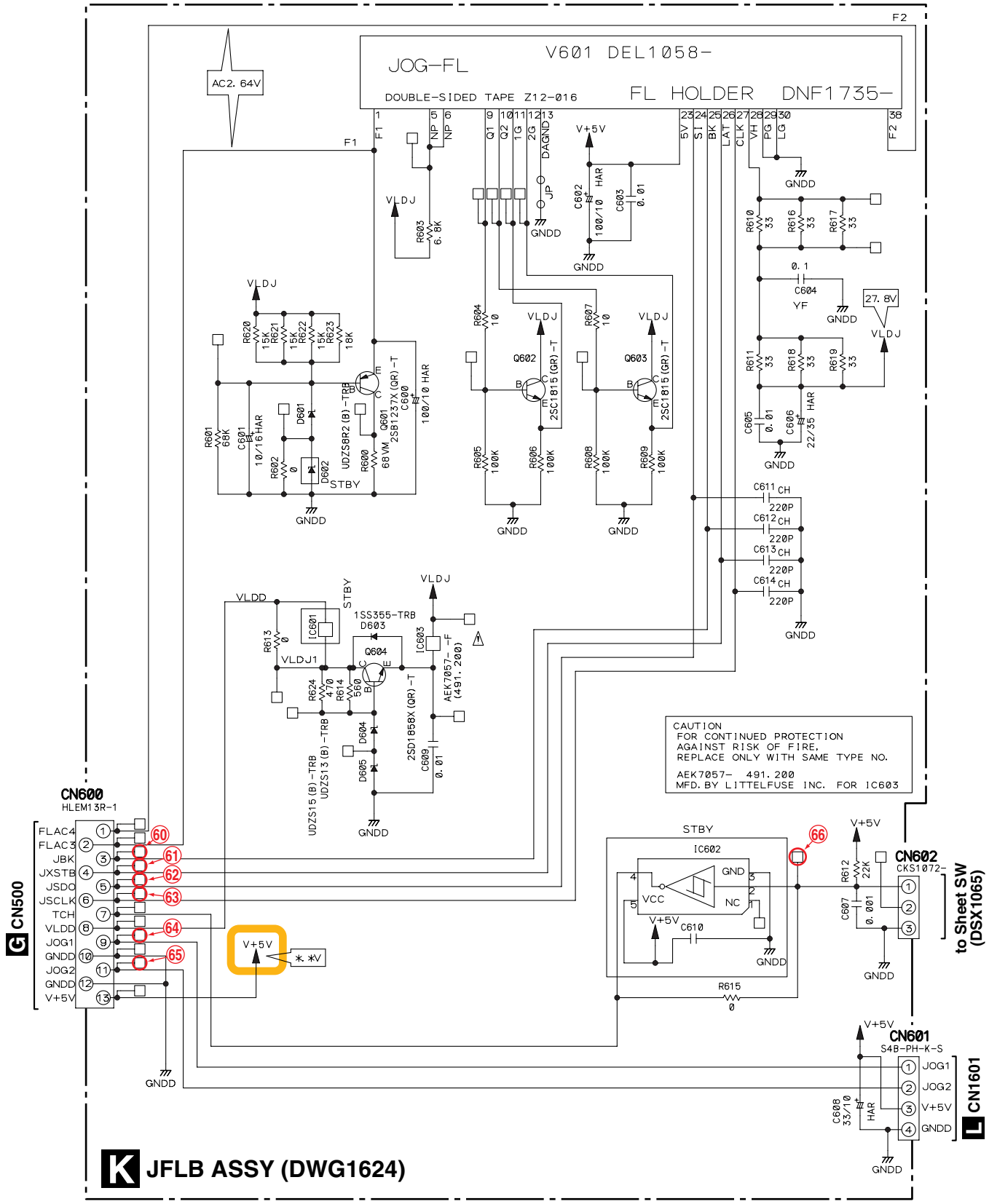
	KUCXJ	WYXJ5	RLFXJ
ASSY	DWM2234	DWM2233	DWM2236
TRNS	DWR1371	DWR1371	DWR1428
ACIN	DWR1430	DWR1429	DWR1432
S2			DSA1026-
AN1	XKP3042-	XKP3041-	XKP3041-
TRANS	DTT1204	DTT1203	←
AC CORD	ADG7021-	ADG1154-	ADG1154- ADG7097-
FU8001	1.6A AEK7075	0.8A REK1021	0.8A REK1021
J2	DKP3621-	DKP3621-	
J3			DKP3620-
CN1	B2P3-VH	B2P3-VH	B3P5-VH


C SECB ASSY (DWR1309)
F REGB ASSY
CN51
CN52
CN53
CN56
CN50
J91
IC51
IC52
IC53
IC54
IC56
IC57
IC58
IC59
IC60
IC61
IC91
IC92
NJM2374AM-TFB
TC7S04FU-TLB
BA00BC0WCP-V5
BA50BC0WFP-TLB
-7V D-D CONVERTER
REGULATOR PLATE DNH2707-
SCREW BBZ30P060FTC
CABLE HOLDER 51048-0600
HEAT SINK VNH1074-
PCB BINDER VEF1040
I CN802
G CN501
A 2/3 CN301
JA51 RKN1004- CONTROL
JA52 AKN7003- DATA IN/OUT
(Data) : AUDIO DATA (Digital)
: The Power supply is shown with the marked box.
CAUTION
FOR CONTINUED PROTECTION
AGAINST RISK OF FIRE,
REPLACE ONLY WITH SAME TYPE NO.
AEK7023- 491.200
MFD. BY LITTELFUSE INC. FOR IC58, 59, 60
AEK7008- 491.800
MFD. BY LITTELFUSE INC. FOR IC53, 61
AEK7065- 4901.5
MFD. BY LITTELFUSE INC. FOR IC54
AEK7009- 491001.
MFD. BY LITTELFUSE INC. FOR IC56


G DFLB ASSY (DWG1623)
V501
DEL1059-(DATA-FL)
FL HOLDER DNF1736-
DOUBLE-SIDED TAPE
Z12-016
CN501
52492-1720
CN56
from SECB
(CN56)
IC501
PEG237A-K
MASK
DISP-CPU
(M30302MCP-***FP)
(FLASH···M30626FHPFP-K)
3→5 CHANGE
TC7SET08FUS1-TLB
IC503
BU4242G-TRB
IC502
RESET IC
DSS1149-T
16MHz
X501
IN/
REALTIME
CUE
(AMBER)
OUT/
OUT ADJ
(AMBER)
B1
(AMBER)
B2
(AMBER)
B4
(AMBER)
B8
(AMBER)
QUICK
RETURN
(GREEN)
REVERSE
(RED)
RELOOP
(AMBER)
IN
4.7K
OUT
4.7K
RELOOP
4.7K
REVERSE
4.7K
FLD-
FLD+
QRTN
CALL>
CALL<
MEMORY
DELETE
TEXT
TMODE
STBY
(Data)
(Data)
CNVSS
XRST
BUSY
RXD
TSCLK
TSDO
TSCS
TSDI
XRST
FLAC4
FLAC3
FLAC1
FLAC2
RELOOPL
JBK
JXSTB
FLBK
FLLAT
CLED
PLED
OUTL
KEY0
PLAY
CUE
V7AL
PLED
CLED
AC4.0V
29.3V
VLDD
V+5V
V5AD
GNDD
GAD
KEY2
DP


H KSWB ASSY (DWS1386)
CN502
KP200IB8L
CN1502
AKM7032-
KEY0
PLAY
CUE
GNDAD
GND
V7AL
PLED
CLED
S1501
S1502
S1503
S1504
S1505
S1506
DSG1079- -T
VSG1024- -T
T-SEARCH-R
T-SEARCH-F
SEARCH-R
SEARCH-F
R1501 3.3K
R1502 3.9K
R1503 5.6K
GNDD1
V7A
C1501
STBY GAD1
2SC4081 (RS) -TLB
SLI-343YCW (RST) -TS
D1502
D1503
Q1502
TLGE68TG (NP) -TS
R1504 22K
R1505 270
R1506 22K
R1507 270
D1501
D1504
CUE (AMBER)
PAUSE PLAY/ (GREEN)
CN500
52492-1320
V+5V
GNDD
JOG2
JOG1
VLDD
TCH
JSCLK
JSDO
JXSTB
JBK
FLAC3
FLAC4
to JFLB (CN600)
K CN600
Notes
RESISTORS NO MARK : RS1/16S***J
RN : RN1/16SE****D
CAPACITOR NO MARK : CKSRYB µF
CH : CCSRCH F
HAR : CEHAR µF
HAT : CEHAT µF
M : CQMBA µF
YF : CKSRYF µF
STBY is STANBY.
I JACK ASSY (DWG1626)
V+8A1
AUDIO FILTER
C805 100/16 HAT
R805 10K
R806 11K RN
L3
C802
IC801 (2/2) NJM4558DX
R808 1K
R809 0
L4
STBY
C812
JA801 DKB1053-
AUDIO OUT
L
R
R814 0
R818 0
C810
C811
CN801
VKN1240-
LOUT
GNDA
GNDA
ROUT
V+8A
MUTE
V-7A
GND
DOUT
A 3/3 CN701
from MAIN (CN701)
GNDO
R801 470
R802 3.3K
D801 1SS355-TRB
Q801
C801 0.001
C806 0.0015
C808 0.0015
C807 0.1
C832 100/16 HAT
R807 27K
R810 1.2K
Q802
C804 0.001
R803 27K
R832 3.3K
D831 1SS355-TRB
Q831
C831 0.001
C838 0.0015
R833 27K
R840 1.2K
Q832
GNDJ
R831 470
R816 470
R841 1.8K
R834 1.8K
IC801 NJM4558DX (1/2)
C833 100/16 HAT
R838 1K
R839 0
C834 0.001
C809 0.1
R820 0
R821 22K
JA802 PKB1033-
1=DOUT
2=GND
D-OUT
C813
GNDO
STBY
R1
R2
R3
R4
C836 0.0015
R835 10K
R836 11K RN
-6.8V
V-7A1
C CN50
CN802
B3B-PH-K-S
V+8A
V+8A
V-7A
to SECB (CN50)
PCB BINDER VEF1040-
FLASH UPDATE
D515
1SS355-TRB
CNVSS
XRST
GND
BUSY
VCC
SCLK
RXD
TXD
FLSCLK
FLSDO
EARTH PLATE
V5AD
CN503
VKN1363-
GNDF
V5AD
ADIN
ADCT
GNDAD
JVOL
KEY1SL
VINL
MTL
TEMPOL
GNDF
GNDF TEMPO
TEMPOR
TCH/R
GAD
to SLDB (CN1503)
J CN1503
: The Power supply is shown with the marked box.
(Data) : PANEL DATA (Digital)
(Ana) : AUDIO Lch OUT (Analog)
: DIGITAL AUDIO OUT (Digital)

3.10 JFLB, SLDB, SLMB and JOGB ASSYS



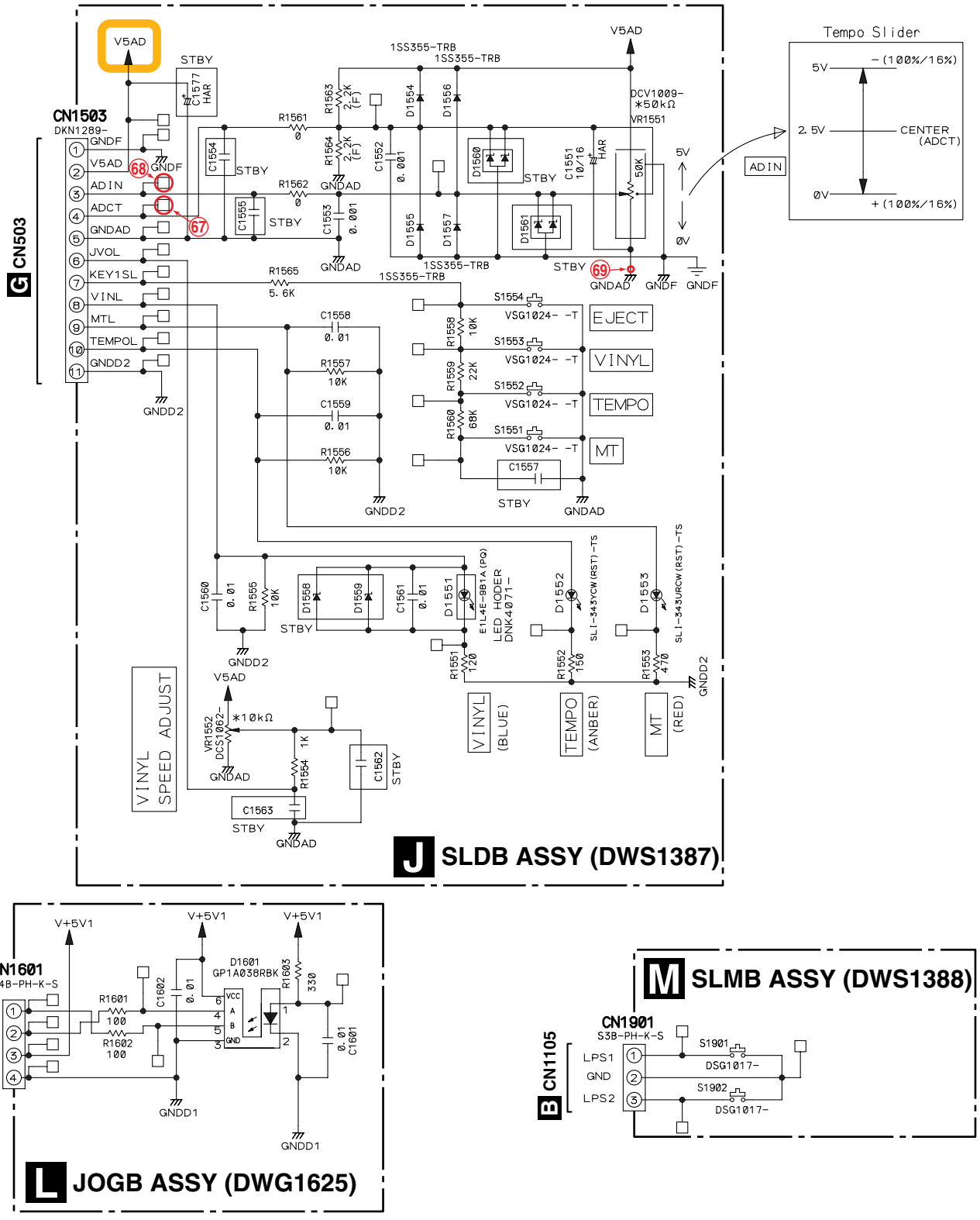
Notes

RESISTORS	NO MARK	: RS1/16S***J
	F	: RS1/16S****F
	VM	: RD1/2VM***J
CAPACITOR	NO MARK	: CKSRYB μF
	YF	: CKSRYF μF
	CH	: CCSRCH F
	HAR	: CEHAR μF

STBY is STANBY.

The ⚠ mark found on some component parts should be replaced with same parts (safety regulation authorized) of identical designation.

: The Power supply is shown with the marked box.

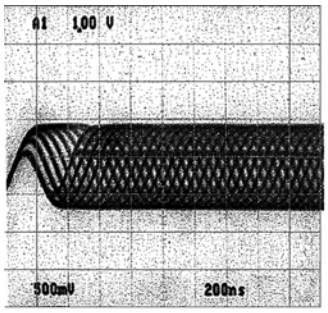


3.11 WAVEFORMS

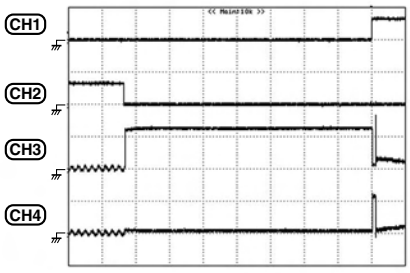
Note: The numbers for the waveform photos (circled) are identical to those for the schematic diagrams, PCB diagrams, and troubleshooting flowcharts.

A MAIN ASSY

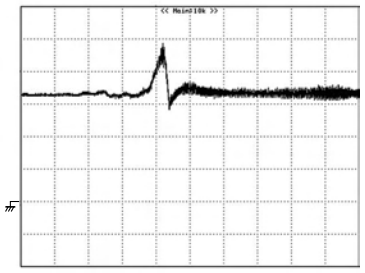
CD player
RF eye pattern waveform (RFO)
① **CH1 : RFO**
V: 500 mV/div. H: 200 nsec/div.



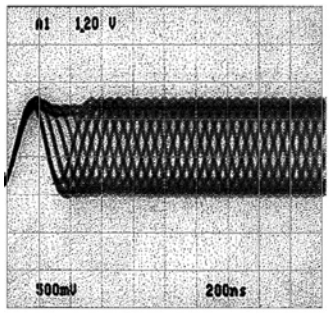
CD player
Load in (2/2)
③ **CH1 : LPS1**
V: 5.0 V/div. H: 100 msec/div.
④ **CH2 : LPS2**
V: 5.0 V/div. H: 100 msec/div.
⑥ **CH3 : LO+**
V: 5.0 V/div. H: 100 msec/div.
⑦ **CH4 : LO–**
V: 5.0 V/div. H: 100 msec/div.



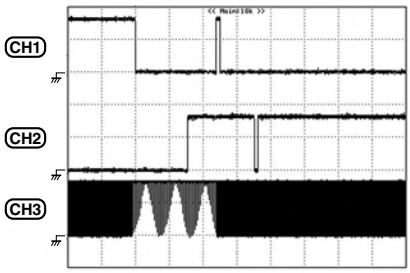
CD player
Focus in (1/2)
⑧ **CH1 : FE**
V: 0.5 V/div. H: 2 msec/div.



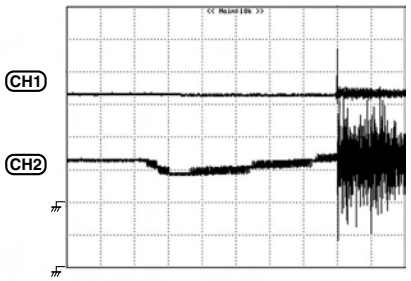
CD player
RF eye pattern waveform (AGCRF)
② **CH1 : AGCRF**
V: 500 mV/div. H: 200 nsec/div.



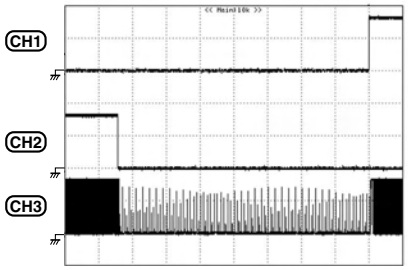
CD player
Load out (1/2)
③ **CH1 : LPS1**
V: 2.0 V/div. H: 500 msec/div.
④ **CH2 : LPS2**
V: 2.0 V/div. H: 500 msec/div.
⑤ **CH3 : PWMLO**
V: 2.0 V/div. H: 500 msec/div.



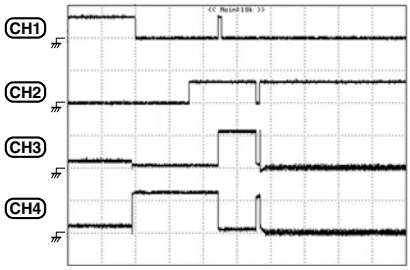
CD player
Focus in (2/2)
⑧ **CH1 : FE**
V: 0.5 V/div. H: 100 msec/div.
⑨ **CH2 : FOO**
V: 0.5 V/div. H: 100 msec/div.



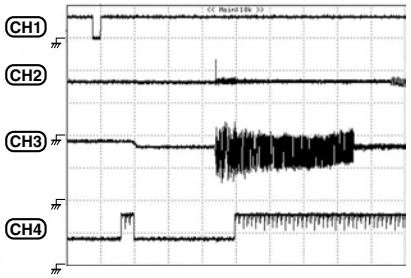
CD player
Load in (1/2)
③ **CH1 : LPS1**
V: 2.0 V/div. H: 100 msec/div.
④ **CH2 : LPS2**
V: 2.0 V/div. H: 100 msec/div.
⑤ **CH3 : PWMLO**
V: 2.0 V/div. H: 100 msec/div.



CD player
Load out (2/2)
③ **CH1 : LPS1**
V: 5.0 V/div. H: 500 msec/div.
④ **CH2 : LPS2**
V: 5.0 V/div. H: 500 msec/div.
⑥ **CH3 : LO+**
V: 5.0 V/div. H: 500 msec/div.
⑦ **CH4 : LO–**
V: 5.0 V/div. H: 500 msec/div.



CD player
Start up
⑩ **CH1 : INSIDE**
V: 5.0 V/div. H: 200 msec/div.
⑧ **CH2 : FE**
V: 1.0 V/div. H: 200 msec/div.
⑪ **CH3 : TE**
V: 1.0 V/div. H: 200 msec/div.
⑫ **CH4 : DMO**
V: 2.0 V/div. H: 200 msec/div.



A MAIN ASSY

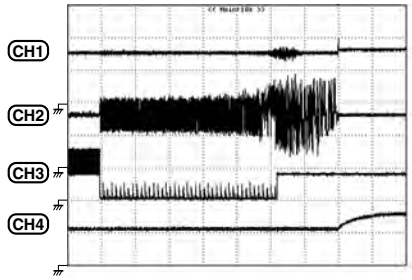
CD player
Stop

(8) **CH1 : FE**
V: 1.0 V/div. H: 200 msec/div.

(11) **CH2 : TE**
V: 1.0 V/div. H: 200 msec/div.

(12) **CH3 : DMO**
V: 2.0 V/div. H: 200 msec/div.

(13) **CH4 : LDO**
V: 2.0 V/div. H: 200 msec/div.



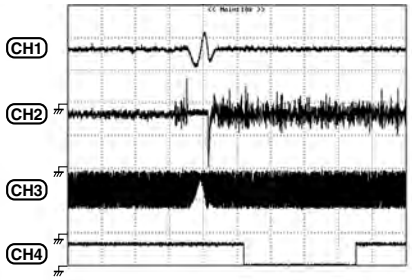
CD player
Pause

(11) **CH1 : TE**
V: 1.0 V/div. H: 1 msec/div.

(14) **CH2 : TRO**
V: 1.0 V/div. H: 1 msec/div.

(1) **CH3 : RFO**
V: 1.0 V/div. H: 1 msec/div.

(17) **CH4 : SBOK**
V: 5.0 V/div. H: 1 msec/div.



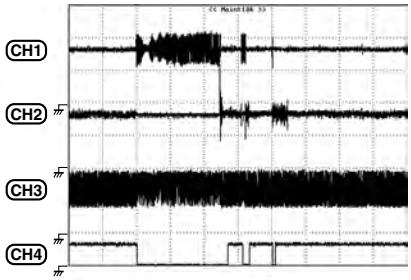
CD player
Track search (1/2)

(11) **CH1 : TE**
V: 1.0 V/div. H: 50 msec/div.

(14) **CH2 : TRO**
V: 1.0 V/div. H: 50 msec/div.

(1) **CH3 : RFO**
V: 1.0 V/div. H: 50 msec/div.

(17) **CH4 : SBOK**
V: 5.0 V/div. H: 50 msec/div.



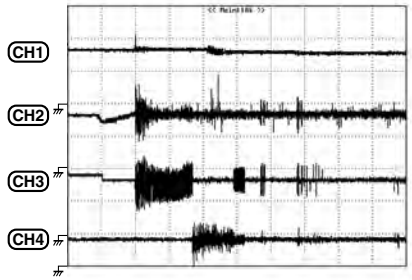
CD player
Auto adjust

(8) **CH1 : FE**
V: 1.0 V/div. H: 500 msec/div.

(9) **CH2 : FOO**
V: 1.0 V/div. H: 500 msec/div.

(11) **CH3 : TE**
V: 1.0 V/div. H: 500 msec/div.

(14) **CH4 : TRO**
V: 2.0 V/div. H: 500 msec/div.



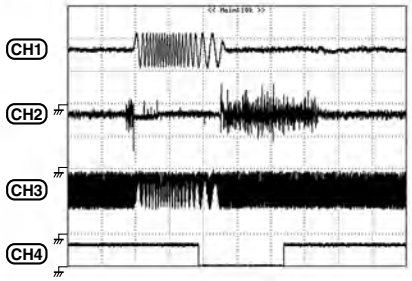
CD player
Scan (1/2)

(11) **CH1 : TE**
V: 1.0 V/div. H: 2 msec/div.

(14) **CH2 : TRO**
V: 1.0 V/div. H: 2 msec/div.

(1) **CH3 : RFO**
V: 1.0 V/div. H: 2 msec/div.

(17) **CH4 : SBOK**
V: 5.0 V/div. H: 2 msec/div.



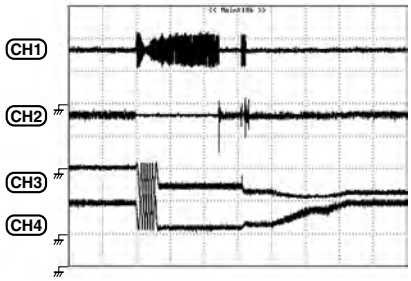
CD player
Track search (2/2)

(8) **CH1 : FE**
V: 1.0 V/div. H: 50 msec/div.

(11) **CH2 : TE**
V: 1.0 V/div. H: 50 msec/div.

(15) **CH3 : SL1IN**
V: 1.0 V/div. H: 50 msec/div.

(16) **CH4 : SL2IN**
V: 1.0 V/div. H: 50 msec/div.



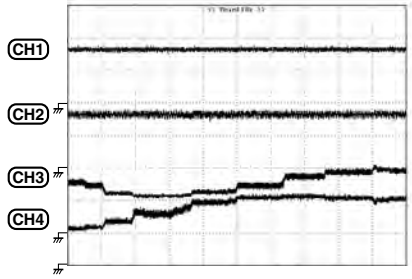
CD player
Play

(8) **CH1 : FE**
V: 1.0 V/div. H: 500 msec/div.

(11) **CH2 : TE**
V: 1.0 V/div. H: 500 msec/div.

(15) **CH3 : SL1IN**
V: 1.0 V/div. H: 500 msec/div.

(16) **CH4 : SL2IN**
V: 1.0 V/div. H: 500 msec/div.



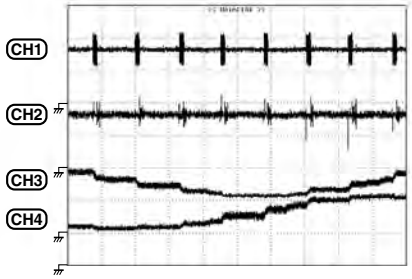
CD player
Scan (2/2)

(8) **CH1 : FE**
V: 1.0 V/div. H: 50 msec/div.

(11) **CH2 : TE**
V: 1.0 V/div. H: 50 msec/div.

(15) **CH3 : SL1IN**
V: 1.0 V/div. H: 50 msec/div.

(16) **CH4 : SL2IN**
V: 1.0 V/div. H: 50 msec/div.



Reset system in the core block

(18) **CH1 : RST** from Reset IC to CPU
V: 5.0 V/div. H: 200 msec/div.

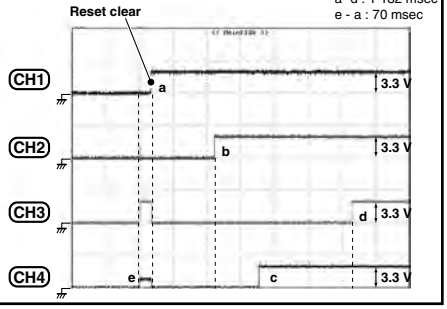
(19) **CH2 : PRGM** from CPU to FPGA through IC312
V: 5.0 V/div. H: 200 msec/div.

(20) **CH3 : SRVRST** from CPU to IC101
V: 5.0 V/div. H: 200 msec/div.

(21) **CH4 : DSPRST** from CPU to IC701
V: 5.0 V/div. H: 200 msec/div.

Conditions: At the time of power on, without a disc loaded

a - b : 370 msec
a - c : 636 msec
a -d : 1 182 msec
e - a : 70 msec



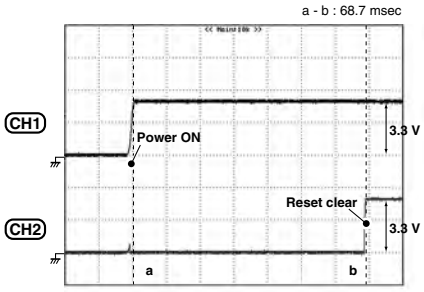
A MAIN ASSY

MPU
Delay time of Reset IC (IC304)

(22) **CH1 : V+3D**
V: 2.0 V/div. H: 10 msec/div.

(18) **CH2 : RST** from Reset IC to CPU
V: 2.0 V/div. H: 10 msec/div.

Conditions: At the time of power on, without a disc loaded
Remark: Set value for reset delay time: 70 msec



FPGA
Configuration (2/3)

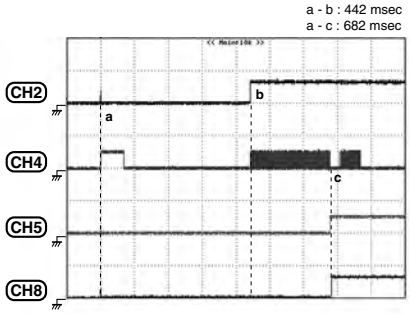
(24) **CH2 : XINIT** to CPU
V: 5.0 V/div. H: 100 msec/div.

(26) **CH4 : DATA** from CPU
V: 5.0 V/div. H: 100 msec/div.

(27) **CH5 : DONE** to CPU
V: 5.0 V/div. H: 100 msec/div.

(30) **CH8 : XFRST** from CPU
V: 5.0 V/div. H: 100 msec/div.

Conditions: At the time of power on, without a disc loaded



Audio DSP
Configuration (2/2)

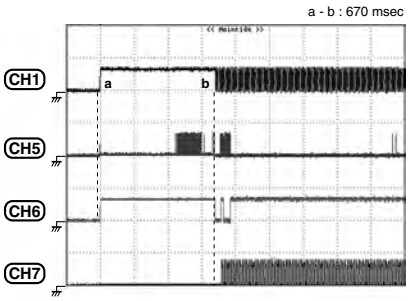
(29) **CH1 : DSP16M** from FPGA
V: 5.0 V/div. H: 200 msec/div.

(26) **CH5 : DATA** from CPU
V: 5.0 V/div. H: 200 msec/div.

(34) **CH6 : DSPDREQ** to FPGA & CPU
V: 5.0 V/div. H: 200 msec/div.

(35) **CH7 : DAC11M** to IC702
V: 5.0 V/div. H: 200 msec/div.

Conditions: At the time of power on, without a disc loaded



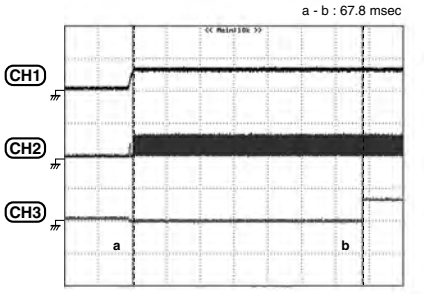
MPU
Association between the 16.93 MHz clock signal and resetting of the MPU

(22) **CH1 : V+3D**
V: 5.0 V/div. H: 10 msec/div.

(71) **CH2 : CPU16M** from IC310 to CPU
V: 5.0 V/div. H: 10 msec/div.

(18) **CH3 : RST** from Reset IC to CPU
V: 5.0 V/div. H: 10 msec/div.

Conditions: At the time of power on, without a disc loaded



FPGA
Configuration (3/3)

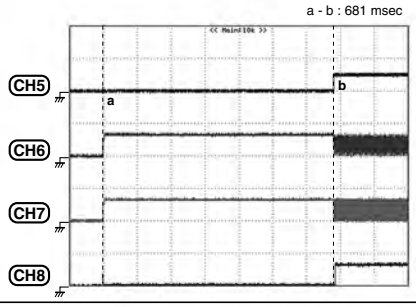
(27) **CH5 : DONE** to CPU
V: 5.0 V/div. H: 100 msec/div.

(28) **CH6 : SRV16M** to IC101
V: 5.0 V/div. H: 100 msec/div.

(29) **CH7 : DSP16M** to IC701
V: 5.0 V/div. H: 100 msec/div.

(30) **CH8 : XFRST** from CPU
V: 5.0 V/div. H: 100 msec/div.

Conditions: At the time of power on, without a disc loaded



Servo DSP
Configuration (1/2)

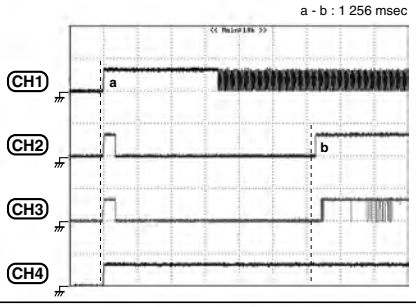
(28) **CH1 : SRV16M** from FPGA
V: 5.0 V/div. H: 200 msec/div.

(20) **CH2 : SRVRST** from CPU
V: 5.0 V/div. H: 200 msec/div.

(36) **CH3 : SRVBUS0** CPU - SRV
V: 5.0 V/div. H: 200 msec/div.

(37) **CH4 : DRVMUTE1** from CPU to IC102
V: 5.0 V/div. H: 200 msec/div.

Conditions: At the time of power on, without a disc loaded



FPGA
Configuration (1/3)

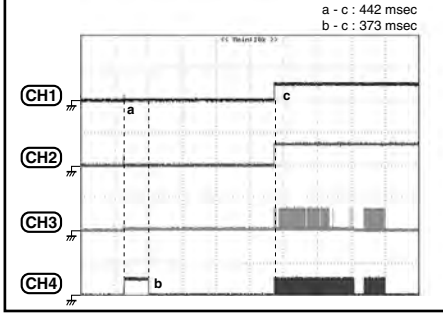
(23) **CH1 : PROG_B (IC302 - pin 99)** from CPU to FPGA
V: 5.0 V/div. H: 100 msec/div.

(24) **CH2 : XINIT** to CPU
V: 5.0 V/div. H: 100 msec/div.

(25) **CH3 : CLK** from CPU to FPGA
V: 5.0 V/div. H: 100 msec/div.

(26) **CH4 : DATA** from CPU
V: 5.0 V/div. H: 100 msec/div.

Conditions: At the time of power on, without a disc loaded



Audio DSP
Configuration (1/2)

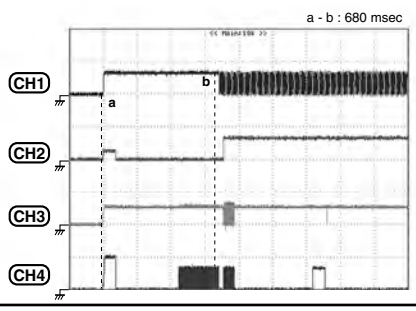
(29) **CH1 : DSP16M** from FPGA
V: 5.0 V/div. H: 200 msec/div.

(21) **CH2 : DSPRST** from CPU
V: 5.0 V/div. H: 200 msec/div.

(31) **CH3 : DSPSIN** to CPU
V: 5.0 V/div. H: 200 msec/div.

(32) **CH4 : CLK** from CPU
V: 5.0 V/div. H: 200 msec/div.

Conditions: At the time of power on, without a disc loaded



Servo DSP
Configuration (2/2)

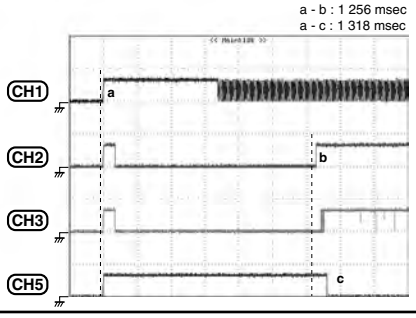
(28) **CH1 : SRV16M** from FPGA
V: 5.0 V/div. H: 200 msec/div.

(20) **CH2 : SRVRST** from CPU
V: 5.0 V/div. H: 200 msec/div.

(36) **CH3 : SRVBUS0** CPU - SRV
V: 5.0 V/div. H: 200 msec/div.

(38) **CH5 : DRVMUTE2** from CPU to IC102
V: 5.0 V/div. H: 200 msec/div.

Conditions: At the time of power on, without a disc loaded



A MAIN ASSY

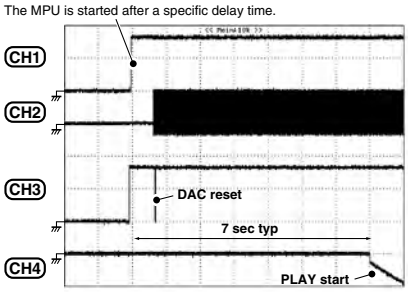
DAC
DAC reset

(18) **CH1 : RST** from CPU Reset IC
V: 2.0 V/div. H: 1 sec/div.

(35) **CH2 : DAC11M** from AUDIO DSP
V: 5.0 V/div. H: 1 sec/div.

(39) **CH3 : DACRST** from CPU IC
V: 2.0 V/div. H: 1 sec/div.

(40) **CH4 : L4 (JACK Assy)** Audio Signal Line
V: 20.0 V/div. H: 1 sec/div.



Audio mute
Association between zero-data detection and muting control (1/2)

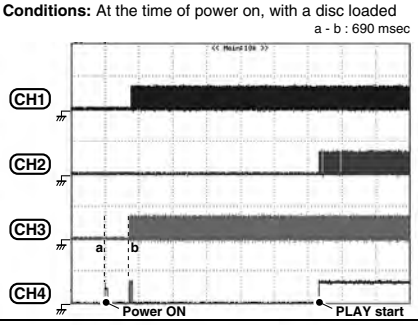
(41) **CH1 : DACLRCK** from DAC
V: 5.0 V/div. H: 1 sec/div.

(42) **CH2 : DACDATA** from DAC
V: 5.0 V/div. H: 1 sec/div.

(43) **CH3 : DACBCK** from DAC
V: 5.0 V/div. H: 1 sec/div.

(44) **CH4 : ZERO** to CPU
V: 5.0 V/div. H: 1 sec/div.

Conditions: At the time of power on, with a disc loaded



Audio mute
Conditions in which muting for zero-data detection is activated (pause, continuous search)

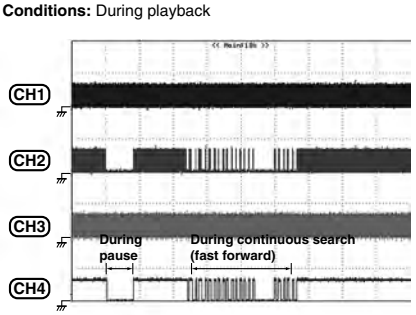
(41) **CH1 : DACLRCK** from DAC
V: 5.0 V/div. H: 1 sec/div.

(42) **CH2 : DACDATA** from DAC
V: 5.0 V/div. H: 1 sec/div.

(43) **CH3 : DACBCK** from DAC
V: 5.0 V/div. H: 1 sec/div.

(44) **CH4 : ZERO** to CPU
V: 5.0 V/div. H: 1 sec/div.

Conditions: During playback



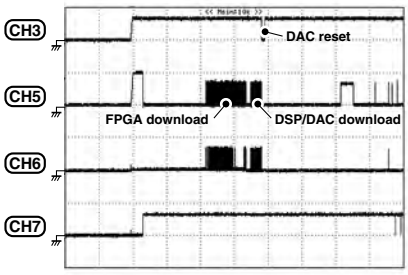
DAC
Initialization of DAC (downloading using the common 3-wire serial lines)

(39) **CH3 : DACRST** from CPU IC
V: 5.0 V/div. H: 200 msec/div.

(32) **CH5 : CLK** from CPU IC
V: 5.0 V/div. H: 200 msec/div.

(26) **CH6 : DATA** from CPU IC
V: 5.0 V/div. H: 200 msec/div.

(33) **CH7 : DACCS** from CPUIC
V: 5.0 V/div. H: 200 msec/div.



Audio mute
Association between zero-data detection and muting control (2/2)

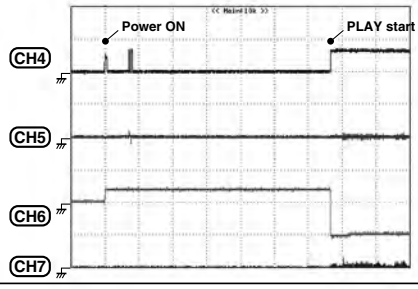
(44) **CH4 : ZERO** to CPU
V: 5.0 V/div. H: 1 sec/div.

(45) **CH5 : L ch** to JACK Assy
V: 5.0 V/div. H: 1 sec/div.

(46) **CH6 : MUTE** to JACK Assy
V: 5.0 V/div. H: 1 sec/div.

(47) **CH7 : L ch (JACK Assy)**
V: 5.0 V/div. H: 1 sec/div.

Conditions: At the time of power on, with a disc loaded



Audio mute
Conditions in which muting for zero-data detection is activated (Jog Touch, track search)

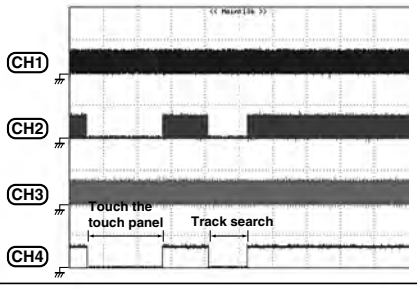
(41) **CH1 : DACLRCK** from DAC
V: 5.0 V/div. H: 1 sec/div.

(42) **CH2 : DACDATA** from DAC
V: 5.0 V/div. H: 1 sec/div.

(43) **CH3 : DACBCK** from DAC
V: 5.0 V/div. H: 1 sec/div.

(44) **CH4 : ZERO** to CPU
V: 5.0 V/div. H: 1 sec/div.

Conditions: During playback



DAC
DAC controlled by the MPU (fixed-cycle polling using the common 3-wire serial lines)

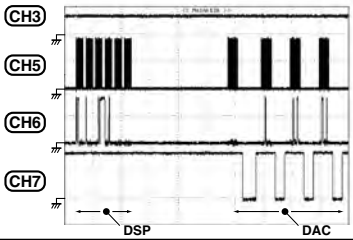
(39) **CH3 : DACRST** from CPU IC
V: 5.0 V/div. H: 5 µsec/div.

(32) **CH5 : CLK** from CPU IC
V: 2.0 V/div. H: 5 µsec/div.

(26) **CH6 : DATA** from CPU IC
V: 2.0 V/div. H: 5 µsec/div.

(33) **CH7 : DACCS** from CPU IC
V: 2.0 V/div. H: 5 µsec/div.

Remarks:
- The MPU polls the audio DSP and DAC in a fixed cycle.
- The intervals of a cycle are 3 msec for playback of a CD-DA, and 10 msec for playback of a signal for MP3.



Audio mute
Conditions in which muting for zero-data detection is activated (Standby)

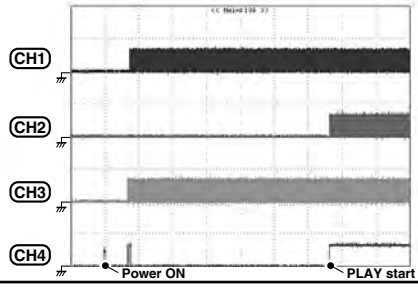
(41) **CH1 : DACLRCK** from DAC
V: 5.0 V/div. H: 1 sec/div.

(42) **CH2 : DACDATA** from DAC
V: 5.0 V/div. H: 1 sec/div.

(43) **CH3 : DACBCK** from DAC
V: 5.0 V/div. H: 1 sec/div.

(44) **CH4 : ZERO** to CPU
V: 5.0 V/div. H: 1 sec/div.

Conditions: At the time of power on, with a disc loaded



Audio mute
Conditions in which muting for zero-data detection is activated (between musical pieces)

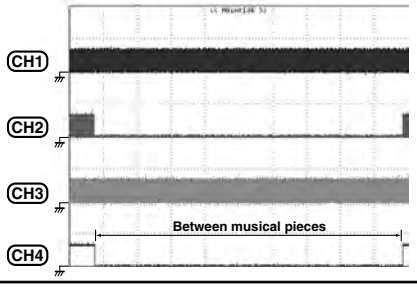
(41) **CH1 : DACLRCK** from DAC
V: 5.0 V/div. H: 1 sec/div.

(42) **CH2 : DACDATA** from DAC
V: 5.0 V/div. H: 1 sec/div.

(43) **CH3 : DACBCK** from DAC
V: 5.0 V/div. H: 1 sec/div.

(44) **CH4 : ZERO** to CPU
V: 5.0 V/div. H: 1 sec/div.

Conditions: During playback



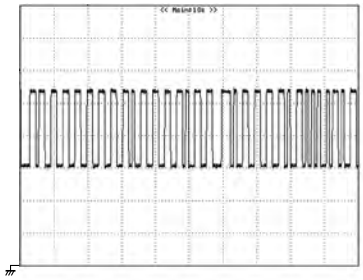
A MAIN ASSY

C SECB ASSY

Digital output
Digital output (on PLAY)

(70) **CH1 : DOUTJ** to JACK Assy
V: 0.5 V/div. H: 2 µsec/div.

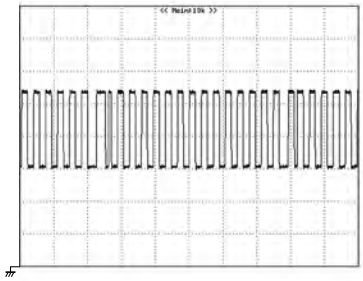
Conditions: During playback



Digital output
Digital output (idle state)

(70) **CH1 : DOUTJ** to JACK Assy
V: 0.5 V/div. H: 2 µsec/div.

Conditions: No disc

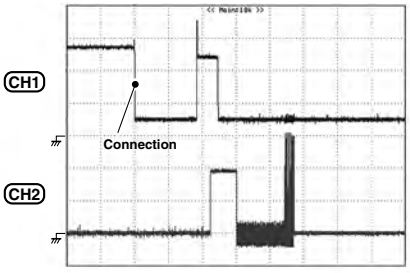


Data copy (DATA IN/OUT terminal)
Detection of connection/disconnection of cables (connection)

(58) **CH1 : RMIN** Detect Line
V: 2.0 V/div. H: 50 msec/div.

(59) **CH2 : JDATA** Data Line
V: 2.0 V/div. H: 50 msec/div.

Conditions: At the time of cable connection

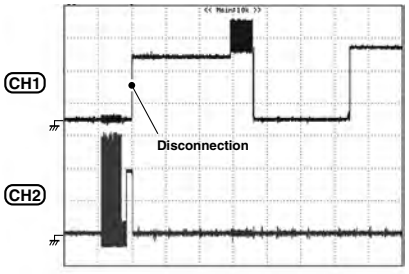


Data copy (DATA IN/OUT terminal)
Detection of connection/disconnection of cables (disconnection)

(58) **CH1 : RMIN** Detect Line
V: 2.0 V/div. H: 5 msec/div.

(59) **CH2 : JDATA** Data Line
V: 2.0 V/div. H: 5 msec/div.

Conditions: At the time of cable disconnection

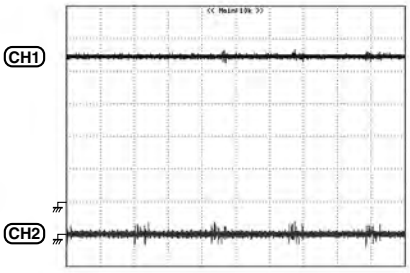


Data copy (DATA IN/OUT terminal)
Detection of connection/disconnection of cables (wireless)

(58) **CH1 : RMIN** Detect Line
V: 1.0 V/div. H: 1 msec/div.

(59) **CH2 : JDATA** Data Line
V: 1.0 V/div. H: 1 msec/div.

Conditions: Wireless, during idling

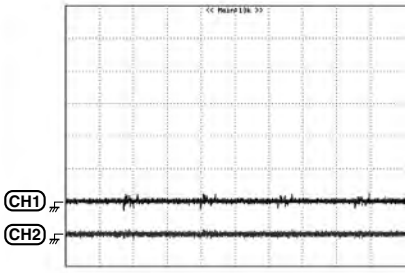


Data copy (DATA IN/OUT terminal)
Detection of connection/disconnection of cables (in a state in which the cables are connected)

(58) **CH1 : RMIN** Detect Line
V: 1.0 V/div. H: 1 msec/div.

(59) **CH2 : JDATA** Data Line
V: 1.0 V/div. H: 1 msec/div.

Conditions: In a state in which the cables are connected, during idling

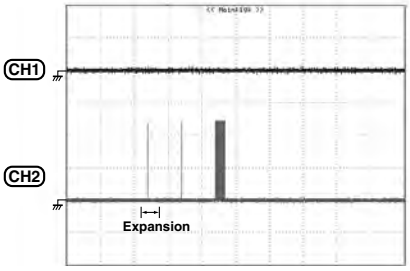


Data copy (DATA IN/OUT terminal)
Data copy

(58) **CH1 : RMIN** Detect Line
V: 2.0 V/div. H: 1 sec/div.

(59) **CH2 : JDATA** Data Line
V: 2.0 V/div. H: 1 sec/div.

Conditions: 10 POINTS × 1 disc

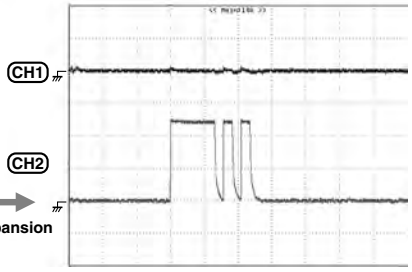


Data copy (DATA IN/OUT terminal)
Data copy (Expansion)

(58) **CH1 : RMIN** Detect Line
V: 2.0 V/div. H: 100 µsec/div.

(59) **CH2 : JDATA** Data Line
V: 2.0 V/div. H: 100 µsec/div.

Conditions: 10 POINTS × 1 disc



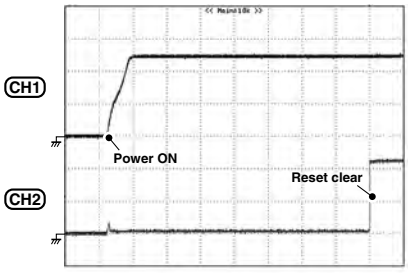
G DFLB ASSY

DISPLAY_MPU
Delay time of Reset IC (IC502)

(48) **CH1 : V+5**
V: 2.0 V/div. H: 10 msec/div.

(49) **CH2 : XRST** to DISP_CPU
V: 2.0 V/div. H: 10 msec/div.

Conditions: At the time of power on, without a disc loaded
Remark: Set value for reset delay time: 70 msec



DISPLAY_MPU
Association between 16 MHz clock signal and resetting of the DISPLAY_MPU

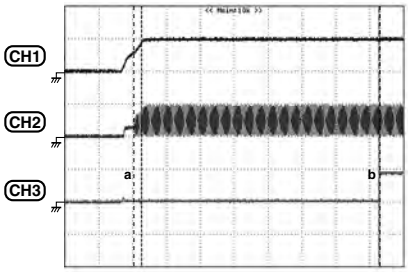
(48) **CH1 : V+5**
V: 5.0 V/div. H: 10 msec/div.

(72) **CH2 : XOUT** to DISP_CPU
V: 5.0 V/div. H: 10 msec/div.

(49) **CH3 : XRST** to DISP_CPU
V: 5.0 V/div. H: 10 msec/div.

Conditions: At the time of power on, without a disc loaded

a - b : 70.10 msec



DISPLAY_MPU
Communication between the FPGA and DISPLAY_MPU (3-wire serial)

(50) **CH1 : TSCLK**
V: 5.0 V/div. H: 200 msec/div.

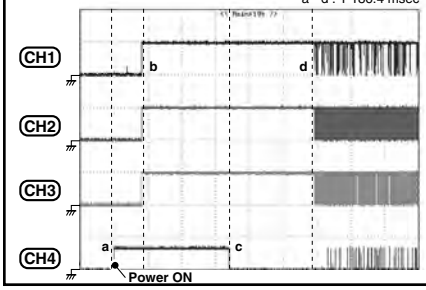
(51) **CH2 : TSCS**
V: 5.0 V/div. H: 200 msec/div.

(52) **CH3 : TSDI**
V: 5.0 V/div. H: 200 msec/div.

(53) **CH4 : TSDO**
V: 5.0 V/div. H: 200 msec/div.

Conditions: At the time of power on, without a disc loaded

a - b : 169.5 msec
a - c : 679.7 msec
a - d : 1 186.4 msec



DATA-FL
Three-wire serial lines (at the time of power on)

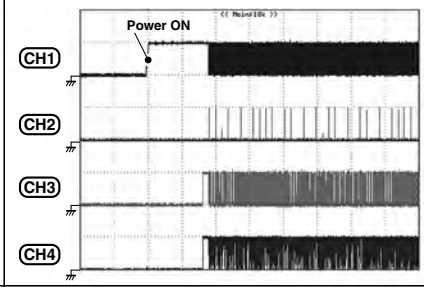
(54) **CH1 : FLBK**
V: 5.0 V/div. H: 100 msec/div.

(55) **CH2 : FLLAT**
V: 5.0 V/div. H: 100 msec/div.

(56) **CH3 : FLSDO**
V: 5.0 V/div. H: 100 msec/div.

(57) **CH4 : FLSCLK**
V: 5.0 V/div. H: 100 msec/div.

Conditions: At the time of power on, without a disc loaded



DATA-FL
Association between the built-in driver and the VLDD power

(73) **CH5 : VLDD**
V: 20.0 V/div. H: 100 msec/div.

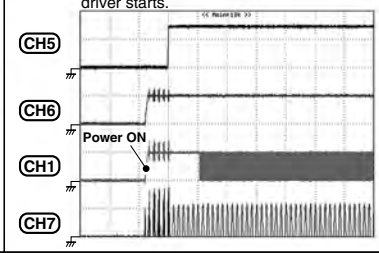
(48) **CH6 : 5V**
V: 5.0 V/div. H: 100 msec/div.

(54) **CH1 : FLBK**
V: 5.0 V/div. H: 100 msec/div.

(74) **CH7 : FLAC1 and FLAC2**
V: 5.0 V/div. H: 100 msec/div.

Conditions: At the time of power on, without a disc loaded

Remark: According to the FL specifications, the Vload power must be stably supplied before the built-in driver starts.



DATA-FL
Three-wire serial lines (during indication on the FL display)

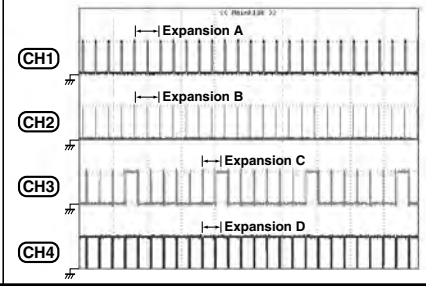
(54) **CH1 : FLBK**
V: 5.0 V/div. H: 1 msec/div.

(55) **CH2 : FLLAT**
V: 5.0 V/div. H: 1 msec/div.

(56) **CH3 : FLSDO**
V: 5.0 V/div. H: 1 msec/div.

(57) **CH4 : FLSCLK**
V: 5.0 V/div. H: 1 msec/div.

Conditions: During playback



J SLDB ASSY

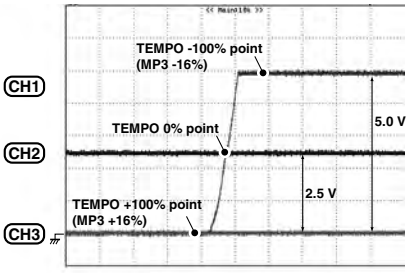
Tempo slider
Slide operation

(68) **CH1 : ADIN** Detect DATA
V: 1.0 V/div. H: 500 msec/div.

(67) **CH2 : ADCT** Compare Level
V: 1.0 V/div. H: 500 msec/div.

(69) **CH3 : GNDAD** GND Level
V: 1.0 V/div. H: 500 msec/div.

Conditions: When the slider is moved from –100% to +100%



K JFLB ASSY

JOG-FL
Three-wire serial lines (At the time of power on)

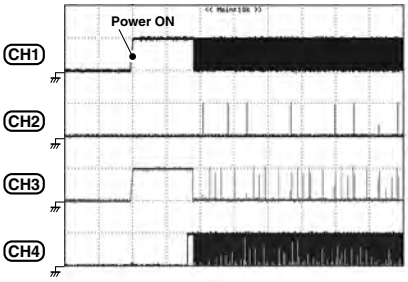
(60) **CH1 : JBK**
V: 5.0 V/div. H: 100 msec/div.

(61) **CH2 : JXSTB**
V: 5.0 V/div. H: 100 msec/div.

(62) **CH3 : JSDO**
V: 5.0 V/div. H: 100 msec/div.

(63) **CH4 : JSCLK**
V: 5.0 V/div. H: 100 msec/div.

Conditions: At the time of power on, without a disc loaded

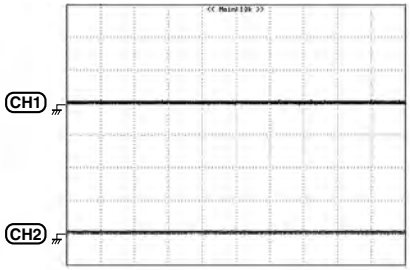


During Jog Dial rotation (encoder process)
Encoder detection (during idling)

(64) **CH1 : JOG1** PHASE1 DATA
V: 2.0 V/div. H: 100 msec/div.

(65) **CH2 : JOG2** PHASE2 DATA
V: 2.0 V/div. H: 100 msec/div.

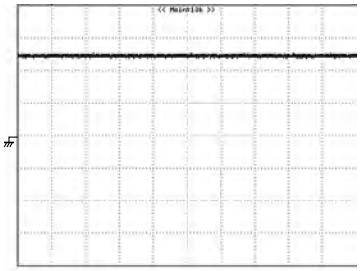
Conditions: Idling



During touch on the Jog plate (detection of pressing force)
Detection of touch (without pressing force)

(66) **CH1 : TCH**
V: 2.0 V/div. H: 10 msec/div.

Conditions: Without pressing force



JOG-FL
Three-wire serial lines (during indication on the FL display, no disc)

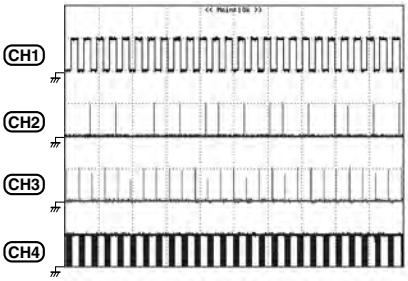
(60) **CH1 : JBK**
V: 5.0 V/div. H: 2 msec/div.

(61) **CH2 : JXSTB**
V: 5.0 V/div. H: 2 msec/div.

(62) **CH3 : JSDO**
V: 5.0 V/div. H: 2 msec/div.

(63) **CH4 : JSCLK**
V: 5.0 V/div. H: 2 msec/div.

Conditions: No disc

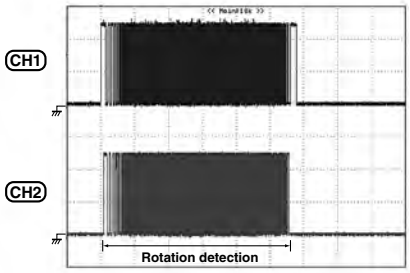


During Jog Dial rotation (encoder process)
Encoder detection (during Jog Dial rotation)

(64) **CH1 : JOG1** PHASE1 DATA
V: 2.0 V/div. H: 100 msec/div.

(65) **CH2 : JOG2** PHASE2 DATA
V: 2.0 V/div. H: 100 msec/div.

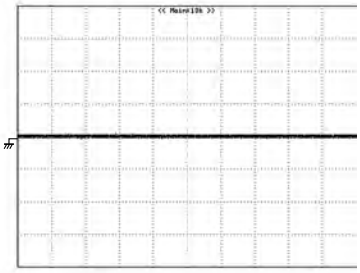
Conditions: During fast rotation



During touch on the Jog plate (detection of pressing force)
Detection of touch (with pressing force)

(66) **CH1 : TCH**
V: 2.0 V/div. H: 10 msec/div.

Conditions: With pressing force



JOG-FL
Three-wire serial lines (during indication on the FL display, during playback)

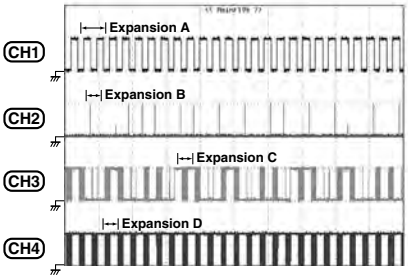
(60) **CH1 : JBK**
V: 5.0 V/div. H: 2 msec/div.

(61) **CH2 : JXSTB**
V: 5.0 V/div. H: 2 msec/div.

(62) **CH3 : JSDO**
V: 5.0 V/div. H: 2 msec/div.

(63) **CH4 : JSCLK**
V: 5.0 V/div. H: 2 msec/div.

Conditions: With a disc loaded, during playback



3.12 VOLTAGES

Note: The voltage measured using the HOZAN DT-113 Digital Tester is an approximation of DC voltage.
Note that the result of measurement of a waveform comprising many AC-current components will vary from tester to tester.

Conditions of measurement:

Play back Track 2 of the STD-905 Test Disc from Pioneer.

- For the IC mounted on the SECB Assy, measurement is performed with loads at the downstream stages lifted.
- The voltage at the MPU (IC301 on the MAIN Assy) is to be measured in Standby mode (not during CD playback), because the unit will freeze up (cannot play back a CD) if the core block is defective.
- As IC303 (SDRAM), IC101 (Servo DSP), IC312 (Logic), IC311 (Logic), IC103 (OP AMP), and IC310 (Logic) are mounted on surface B, measurement is performed with the FFC cable connecting the MAIN and JACK Assys disconnected.

A

MAIN ASSY

IC100 NJM2885DL1-33

Pin No.	Voltage (V)
1	6.0
2	0.00
3	3.3

IC103 NJU7013F

Pin No.	Voltage (V)
1	0.2
2	0.0
3	0.2
4	0.2
5	3.3

IC104 NJM2903M

Pin No.	Voltage (V)
1	3.1
2	1.7
3	1.8
4	0.0
5	1.7
6	1.7
7	1.5
8	3.3

IC105 TC7W04FU

Pin No.	Voltage (V)
1	0.0
2	1.7
3	0.0
4	0.0
5	3.3
6	1.6
7	3.3
8	3.3

IC106 TC7W08FU

Pin No.	Voltage (V)
1	3.3
2	0–3.2
3	0–3.2
4	0.0
5	0–3.2
6	0–3.2
7	0–3.2
8	3.3

IC101 TC94A15FG

Pin No.	Voltage (V)	Pin No.	Voltage (V)
1	0.0	51	1.6
2	2.9–3.3	52	0.0
3	0.0	53	2.4
4	3.3	54	1.6
5	0.0	55	1.5
6	0.0	56	1.8
7	0.0	57	1.7
8	0.0	58	1.6
9	0.0	59	3.3
10	0.0	60	1.6
11	3.3	61	1.6
12	0.0	62	1.6
13	3.3	63	1.6
14	1.6	64	2.0
15	1.6	65	0.0
16	1.6	66	0.0
17	1.6	67	0.7–1.0
18	1.4	68	0.0
19	1.6	69	0.0
20	0.6	70	3.3
21	1.6	71	0.0
22	1.6	72	0.0
23	1.6	73	1.6
24	0.0	74	1.5
25	1.7	75	3.3
26	1.6	76	0.0
27	1.6	77	1.6
28	1.6	78	3.3
29	3.3	79	0.0
30	1.5	80	1.6
31	1.6	81	0.0
32	1.5	82	0.0
33	1.6	83	0.0
34	0.0	84	3.2
35	1.6	85	3.2
36	1.3	86	3.2
37	1.3	87	3.2
38	3.3	88	3.2
39	0.0	89	2.8–3.0
40	3.3	90	3.3
41	2.4	91	3.3
42	0.2	92	1.8–2.4
43	0.0	93	3.3
44	1.8	94	0.0
45	1.7	95	3.3
46	1.7	96	0.0
47	1.7	97	1.7
48	1.8	98	1.7
49	1.8	99	1.7
50	–	100	0.0

IC102 M63018FP

Pin No.	Voltage (V)
1	1.0–2.5
2	1.0–2.5
3	7.1
4	7.1
5	0–7
6	0–7
7	0.0
8	7.1
9	0–7
10	0–7
11	0.0
12	0.5–1.2
13	0.5–1.2
14	0.5–1.2
15	7.1
16	2.5
17	2.5
18	2.5
19	2.5
20	2.5
21	2.5
22	7.1
23	1.7
24	1.6
25	1.7
26	1.7
27	1.7
28	1.7
29	0.0
30	3.1
31	3.1
32	7.1
33	0.0
34	3.1
35	3.1
36	1.1
37	1.1
38	3.3
39	7.1
40	1.7
41	3.3
42	1.1

IC300 DYW1753-B/J

Pin No.	Voltage (V)
1	2.2
2	2.1–2.4
3	0.9–1.2
4	1.7–2.0
5	1.7–1.9
6	1.9–2.2
7	2.0–2.2
8	2.1–2.4
9	0.0
10	0.0
11	2.5–2.8
12	3.3
13	0.0
14	0.0
15	3.3
16	0.5
17	1.2–1.5
18	2.1–2.4
19	2.1–2.4
20	1.8–2.2
21	1.9–2.2
22	1.9–2.2
23	0.9–1.1
24	2.1–2.4
25	1.9
26	3.3
27	0.0
28	3.3
29	0.0
30	3.3
31	0.5–0.8
32	0.5–0.9
33	0.5–0.8
34	0.5–0.8
35	0.5–0.8
36	0.4–0.7
37	3.3
38	0.7–0.8
39	0.6–0.8
40	0.6–0.8
41	0.8–1.0
42	0.5–0.7
43	0.4–0.6
44	0.6–0.7
45	0.5–0.7
46	0.0
47	3.3
48	1.3–1.5

IC301 SCF5249VM140

Pin No.	Voltage (V)	Pin No.	Voltage (V)	Pin No.	Voltage (V)
A1	3.3	F2	0.3	M13	3.2
A2	3.3	F3	3.2	M14	1.5
A3	2.3	F4	0.0	N1	0.7
A4	2.4	F11	0.0	N2	1.2
A5	2.4	F12	0.0	N3	3.0
A6	3.3	F13	3.3	N4	3.3
A7	0.0	F14	0.0	N5	0.0
A8	3.3	G1	0.5	N6	0.6
A9	3.3	G2	0.5	N7	0.4
A10	0.0	G3	0.8	N8	0.0
A11	2.7	G4	0.0	N9	0.0
A12	3.3	G11	3.3	N10	3.3
A13	0.0	G12	0.0	N11	1.7
A14	0.0	G13	0.0	N12	3.3
B1	2.3	G14	0.0	N13	2.5
B2	2.0	H1	0.4	N14	1.7
B3	2.3	H2	0.6	P1	3.0
B4	2.4	H3	0.0	P2	2.6
B5	0.9	H4	0.0	P3	0.0
B6	2.1	H11	1.8	P4	3.3
B7	3.3	H12	3.2	P5	3.3
B8	0.0	H13	3.3	P6	3.3
B9	3.3	H14	1.6	P7	0.6
B10	0.0	J1	0.7	P8	0.5
B11	3.3	J2	0.4	P9	0.0
B12	0.0	J3	3.2	P10	1.5
B13	3.2	J4	0.0	P11	0.0
B14	0.0	J11	0.0	P12	3.3
C1	2.4	J12	3.3	P13	3.3
C2	2.1	J13	0.0	P14	3.3
C3	0.0	J14	0.0		
C4	1.8	K1	0.5		
C11	3.3	K2	2.0		
C12	2.2	K3	0.0		
C13	0.0	K4	0.0		
C14	0.0	K5	0.0		
D1	1.2	K6	1.8		
D2	1.1	K7	0.5		
D3	0.3	K8	3.3		
D4	0.0	K9	0.0		
D5	0.0	K10	0.0		
D6	0.0	K11	0.0		
D7	3.3	K12	0.0		
D8	0.0	K13	0.0		
D9	0.0	K14	0.0		
D10	0.0	L1	0.9		
D11	0.0	L2	2.4		
D12	0.0	L3	3.3		
D13	0.0	L4	3.3		
D14	0.0	L5	3.3		
E1	3.3	L6	3.3		
E2	1.7	L7	4.9		
E3	0.0	L8	0.0		
E4	2.7	L9	4.4		
E5	3.3	L10	1.8		
E6	0.0	L11	0.0		
E7	3.3	L12	3.2		
E8	3.3	L13	1.6		
E9	1.8	L14	3.3		
E10	0.0	M1	2.3		
E11	0.0	M2	0.6		
E12	0.0	M3	0.0		
E13	0.0	M4	0.0		
E14	0.0	M11	3.3		
F1	0.0	M12	0.0		

IC302 XC3S50-4VQG100C

Pin No.	Voltage (V)	Pin No.	Voltage (V)
1	0–1.8	51	2.5
2	1.6	52	0.0
3	0.0	53	2.0
4	3.2	54	1.9–2.2
5	0.0	55	0.0
6	3.3	56	0.0
7	2.5	57	3.3
8	0.0	58	2.5
9	1–4.5	59	0.9
10	0.0	60	2.4
11	1–4.5	61	2.8
12	1.6	62	0.0
13	1.6–1.8	63	3.3
14	1.7	64	3.3
15	1.7	65	0.0
16	1.8	66	0.0
17	1.9	67	1.6
18	1.2	68	1.7
19	3.3	69	1.2
20	0.0	70	3.3
21	0.5–0.7	71	1.6
22	0.5–0.7	72	3.3
23	0.5–0.7	73	0.0
24	2.5	74	3.2
25	2.5	75	0.2
26	2.5	76	2.5
27	0.7–0.9	77	2.5
28	0.7–0.9	78	2.5
29	0.0	79	0.0
30	0.5–0.7	80	2.7
31	3.3	81	0.0
32	0.4–0.7	82	0.0
33	2.5	83	3.3
34	0.6–0.9	84	2.5
35	0.4–0.8	85	0.0
36	0.5–0.7	86	0.0
37	1.6	87	0.0
38	0.5–0.7	88	0.0
39	1.7	89	0.0
40	0.0	90	0.0
41	0.0	91	0.0
42	3.3	92	0.0
43	0.5–0.7	93	1.2
44	0.8–1.0	94	3.3
45	1.2	95	0.0
46	3.3	96	0.0
47	0.6–0.8	97	0.0
48	0.0	98	0.0
49	0.5–0.8	99	2.5
50	0.5–0.8	100	2.5

IC303 K4S641632K-UC75

Pin No.	Voltage (V)
1	3.3
2	0.0
3	3.3
4	0.5–0.7
5	0.6–0.9
6	0.0
7	0.6–0.8
8	0.7–0.8
9	3.3
10	0.6–0.9
11	0.7–0.9
12	0.0
13	0.6–0.8
14	3.3
15	0.0
16	3.0
17	2.6
18	2.8
19	1.2
20	0.9–1.1
21	0.4–0.8
22	0.6
23	0.0
24	2.3
25	0.9–1.1
26	1.7–1.9
27	3.3
28	0.0
29	1.7–1.9
30	1.9–2.2
31	2.0–2.2
32	2.1–2.4
33	1.3–1.6
34	1.2–1.5
35	0.8–1.1
36	0.0
37	3.3
38	1.7
39	0.1
40	0.0
41	0.0
42	0.5–0.7
43	3.3
44	0.5–0.8
45	0.5–0.8
46	0.0
47	3.3
48	0.4–0.7
49	3.3
50	0.8–1.0
51	0.5–0.7
52	0.0
53	0.5–0.8
54	0.0

IC304 BU4230G

Pin No.	Voltage (V)
1	3.3
2	3.3
3	0.0
4	0.0
5	1.7

IC305 MM1561JF

Pin No.	Voltage (V)
1	1.8
2	0.0
3	0.0
4	0.5
5	3.3
6	0.0
7	3.3

IC306 MM1562FF

Pin No.	Voltage (V)
1	2.5
2	0.0
3	0.0
4	1.2
5	3.3
6	0.0
7	3.3

IC307 BD00KA5WFP

Pin No.	Voltage (V)
1	3.3
2	3.3
3	0.0
4	1.2
5	0.8

IC308 TC74VHC08FTS1

Pin No.	Voltage (V)
1	3.3
2	4.8
3	3.2
4	3.3
5	4.3
6	2.9
7	0.0
8	0.0
9	3.3
10	0.0
11	2.7
12	3.3
13	4.0
14	3.3

IC309 TC7SET08FUS1

Pin No.	Voltage (V)
1	4.9
2	3.3
3	0.0
4	4.9
5	4.9

IC310 TC7WU04FU

Pin No.	Voltage (V)
1	1.6
2	1.6
3	1.6
4	0.0
5	1.6
6	1.6
7	1.6
8	3.3

IC311 TC7SH08FUS1

Pin No.	Voltage (V)
1	2.5
2	0.0
3	0.0
4	0.0
5	2.5

IC312 TC7SH08FUS1

Pin No.	Voltage (V)
1	2.5
2	3.3
3	0.0
4	2.5
5	2.5

IC702 PE8001A

Pin No.	Voltage (V)
1	1.6
2	0.0
3	1.6
4	0.0
5	1.6
6	0.0
7	0.0
8	5.0
9	5.0
10	0.0
11	2.5
12	0.0
13	2.5
14	0.0
15	5.0
16	2.5
17	0.0
18	2.5
19	0.0
20	5.0
21	3.3
22	5.0
23	0.0
24	0.0
25	0.0
26	0.0
27	0.0
28	3.3

IC703 BD00KA5WFP

Pin No.	Voltage (V)
1	3.3
2	3.3
3	0.0
4	1.3
5	0.8

IC704 NJM2880U1-05

Pin No.	Voltage (V)
1	8.0
2	0.0
3	1.3
4	5.0
5	8.0

IC701 DSPC56371AF180

Pin No.	Voltage (V)	Pin No.	Voltage (V)
1	0.0	41	3.3
2	0.0	42	0.0
3	3.3	43	0.0
4	0.0	44	1.3
5	0.0	45	1.7–1.8
6	0.0	46	1.2
7	0.8	47	3.3
8	1.3	48	0.6
9	0.0	49	3.3
10	0.0	50	0.6
11	0.0	51	3.3
12	0.0	52	1.3
13	0.0	53	0.0
14	0.0	54	0.0
15	0.0	55	0.0
16	0.0	56	0.0
17	3.3	57	0.0
18	0.0	58	0.0
19	0.0	59	1.0
20	0.0	60	3.2
21	0.0	61	1.6
22	0.0	62	0.0
23	3.3	63	1.7
24	0.0	64	3.3
25	3.3	65	0.0
26	0.0	66	0.0
27	0.0	67	0.0
28	0.0	68	0.0
29	1.3	69	1.6
30	1.1	70	1.6
31	3.0	71	1.3
32	0.0	72	0.0
33	3.0	73	1.6
34	0.0	74	0.0
35	2.6	75	3.3
36	0.0	76	1.7
37	3.3	77	1.6
38	0.0	78	1.6
39	3.3	79	1.6
40	0.0	80	0.0

C

SECB ASSY

IC050 BA00BC0WCP-V5

Pin No.	Voltage (V)
1	12.3
2	12.3
3	0.0
4	8.0
5	1.3

IC051 NJM2374AM

Pin No.	Voltage (V)
1	8.0
2	-2.7
3	-6.1
4	-7.0
5	-5.7
6	8.1
7	8.0
8	8.0

IC052 TC7S04FU

Pin No.	Voltage (V)
1	0.0
2	0.0
3	0.0
4	2.7
5	5.0

IC057 BA50BC0WFP

Pin No.	Voltage (V)
1	8.0
2	8.0
3	0.0
4	5.0
5	0.0

REGB ASSY

IC091 BA00BC0WCP-V5

Pin No.	Voltage (V)
1	6.0
2	6.0
3	0.0
4	3.3
5	1.3

IC092 BA00BC0WCP-V5

Pin No.	Voltage (V)
1	11.2
2	11.2
3	0.0
4	7.2
5	1.3

G

DFLB ASSY

IC501 PEG237B

Pin No.	Voltage (V)	Pin No.	Voltage (V)
1	0.0	51	0.0
2	0.0	52	4.9
3	0.0	53	4.9
4	0.0	54	4.9
5	0.0	55	4.9
6	4.9	56	4.9
7	0.0	57	0.0
8	0.0	58	4.9
9	0.0	59	0.0
10	0.0	60	0.0
11	0.0	61	0.0
12	4.5	62	4.9
13	2.6	63	0.0
14	0.0	64	0.0
15	2.3	65	0.0
16	5.0	66	0.0
17	5.0	67	0.0
18	5.0	68	0.0
19	5.0	69	0.0
20	5.0	70	0.0
21	5.0	71	0.0
22	5.0	72	0.0
23	5.0	73	0.0
24	4.9	74	0.0
25	4.9	75	0.0
26	0.0	76	0.0
27	4.9	77	0.0
28	3.9	78	0.0
29	0.0	79	4.9
30	1.4–1.8	80	4.9
31	0.8	81	4.9
32	4.9	82	4.9
33	4.5	83	4.9
34	4.9	84	4.9
35	4.3	85	4.9
36	0.1	86	4.9
37	4.8	87	4.9
38	4.0	88	4.9
39	4.9	89	2.5
40	0.0	90	2.5
41	0.0	91	4.9
42	0.0	92	4.9
43	0.6	93	4.9
44	0.0	94	4.9
45	2.8	95	4.9
46	4.9	96	0.0
47	0.0	97	0.0
48	4.9	98	4.9
49	4.9	99	4.9
50	0.0	100	4.9

IC502 BU4242G

Pin No.	Voltage (V)
1	4.5
2	4.9
3	0.0
4	0.0
5	2.6

IC503 TC7SET08FUS1

Pin No.	Voltage (V)
1	4.9
2	0.0
3	0.0
4	0.1
5	4.9

I

JACK ASSY

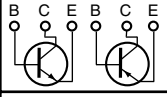
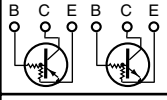
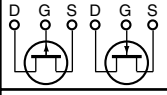
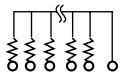
IC801 NJM4558DX

Pin No.	Voltage (V)
1	0.0
2	0.0
3	0.0
4	-6.0
5	0.0
6	0.0
7	0.0
8	8.0

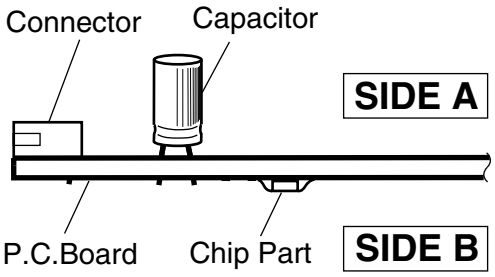
4. PCB CONNECTION DIAGRAM

NOTE FOR PCB DIAGRAMS :

1. Part numbers in PCB diagrams match those in the schematic diagrams.
2. A comparison between the main parts of PCB and schematic diagrams is shown below.

Symbol In PCB Diagrams	Symbol In Schematic Diagrams	Part Name
		Transistor
		Transistor with resistor
		Field effect transistor
		Resistor array
		3-terminal regulator

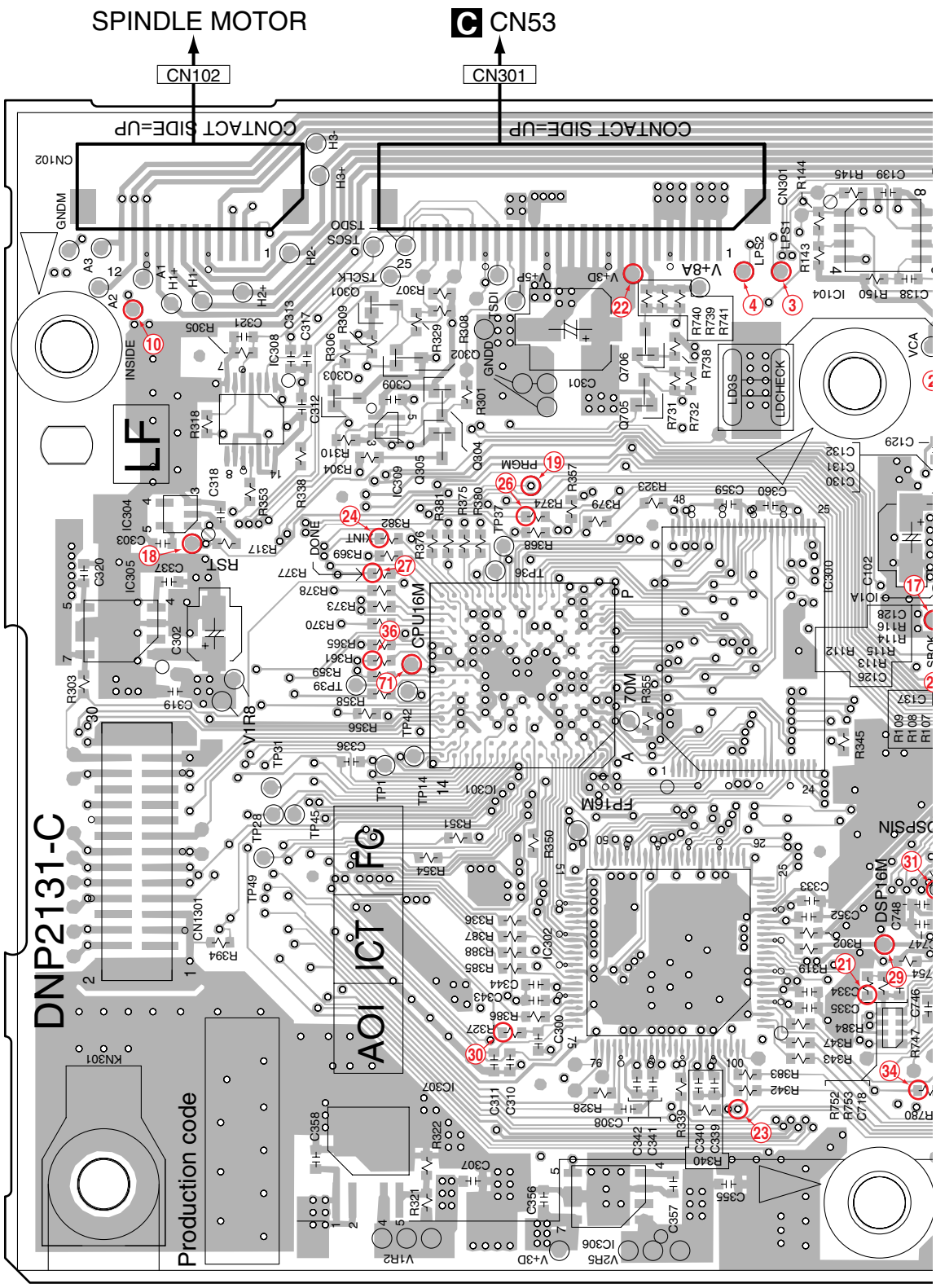
3. The parts mounted on this PCB include all necessary parts for several destinations.
   For further information for respective destinations, be sure to check with the schematic diagram.
4. View point of PCB diagrams.



4.1 MAIN ASSY

SIDE A

A MAIN ASSY

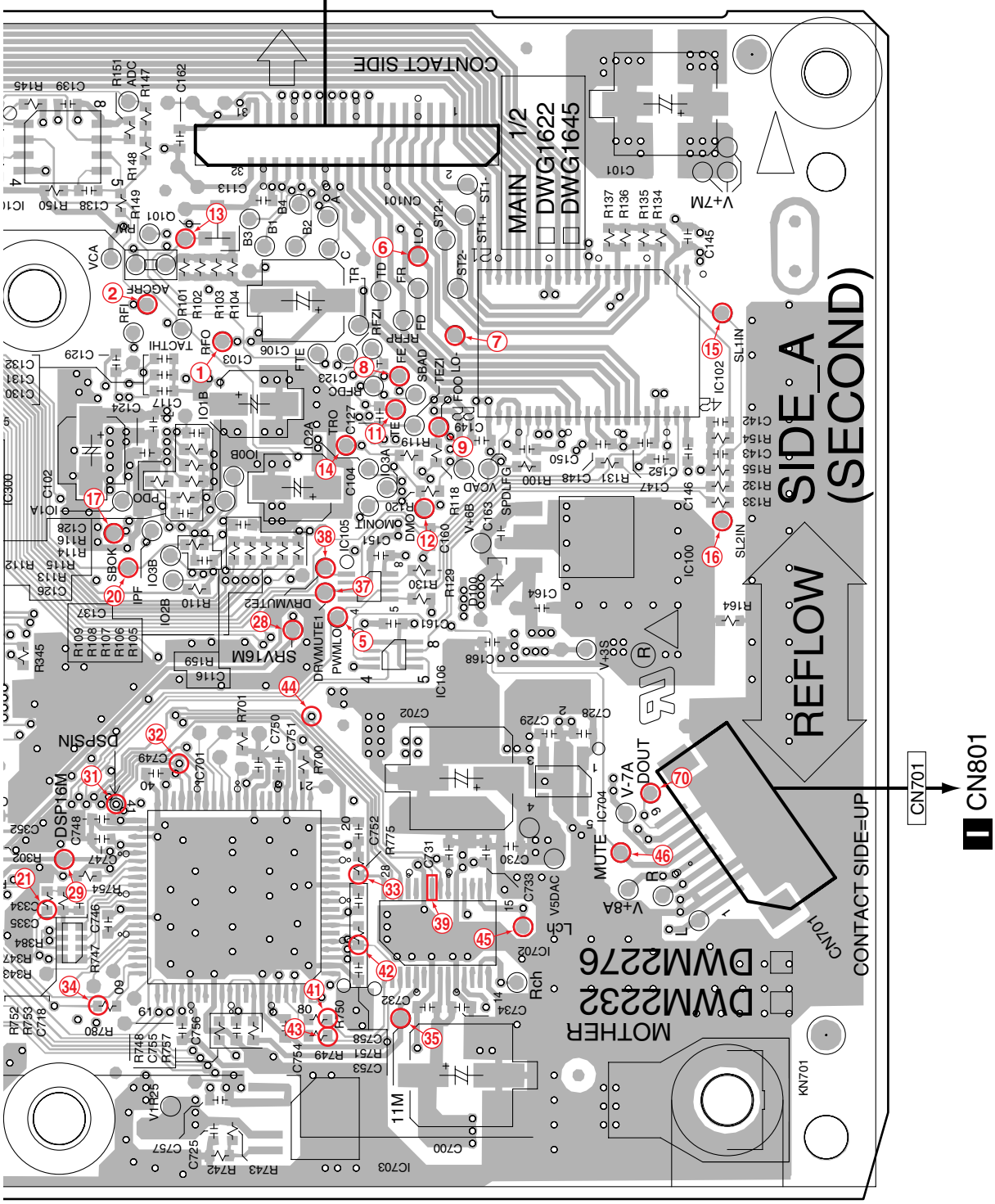


IC304	IC308	Q301	Q305	Q302	IC302	Q706		IC300			
IC305	IC308	Q303	Q305	Q304	IC302	Q705		IC104			
IC304		Q301	IC309	Q302		Q706		IC300			
IC305		Q303	IC309	Q304		Q705		IC104			
				IC307	IC301	IC306					
				IC307	IC301	IC306					

A

B CN1101

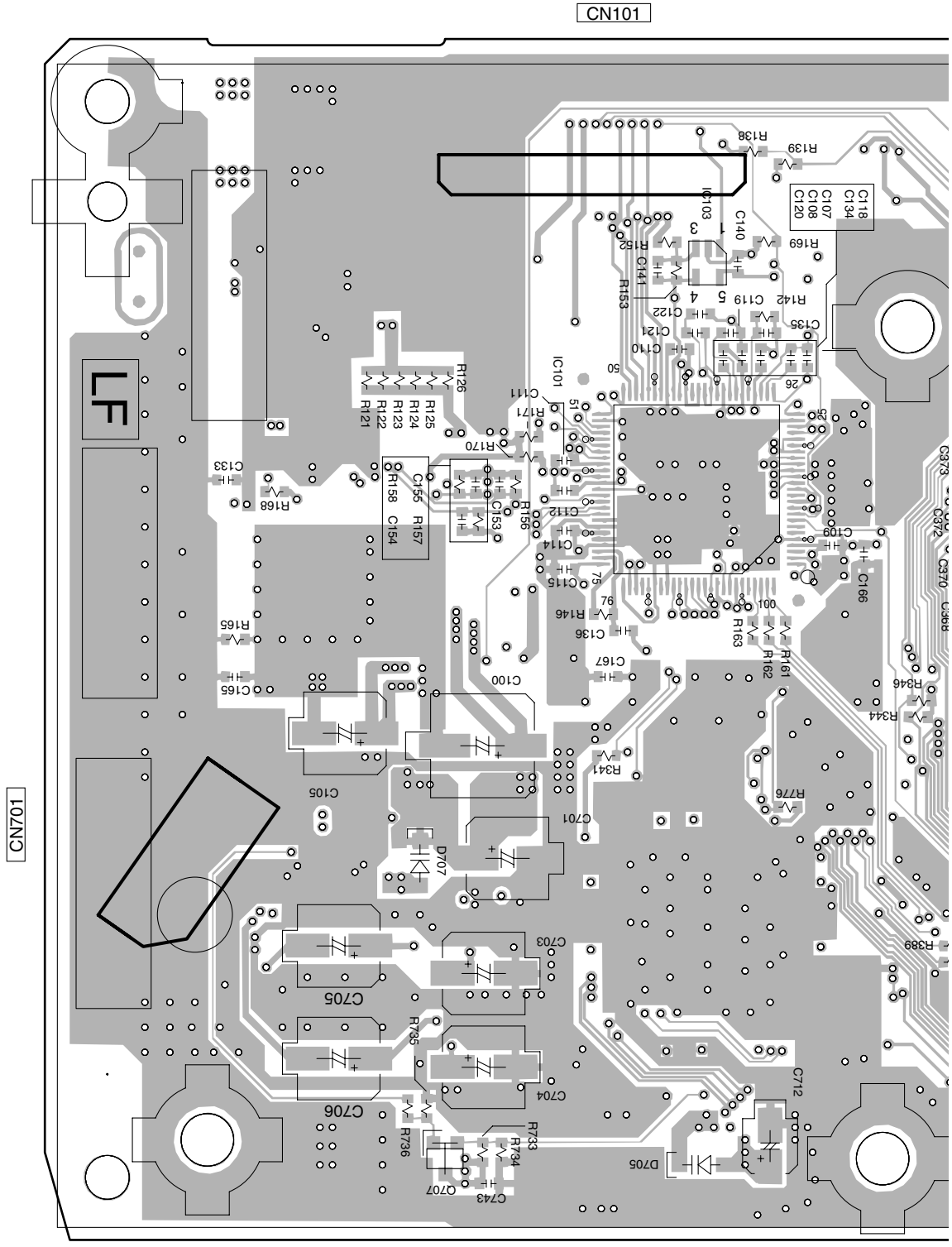
NOTE : The encircled numbers denote measuring point.



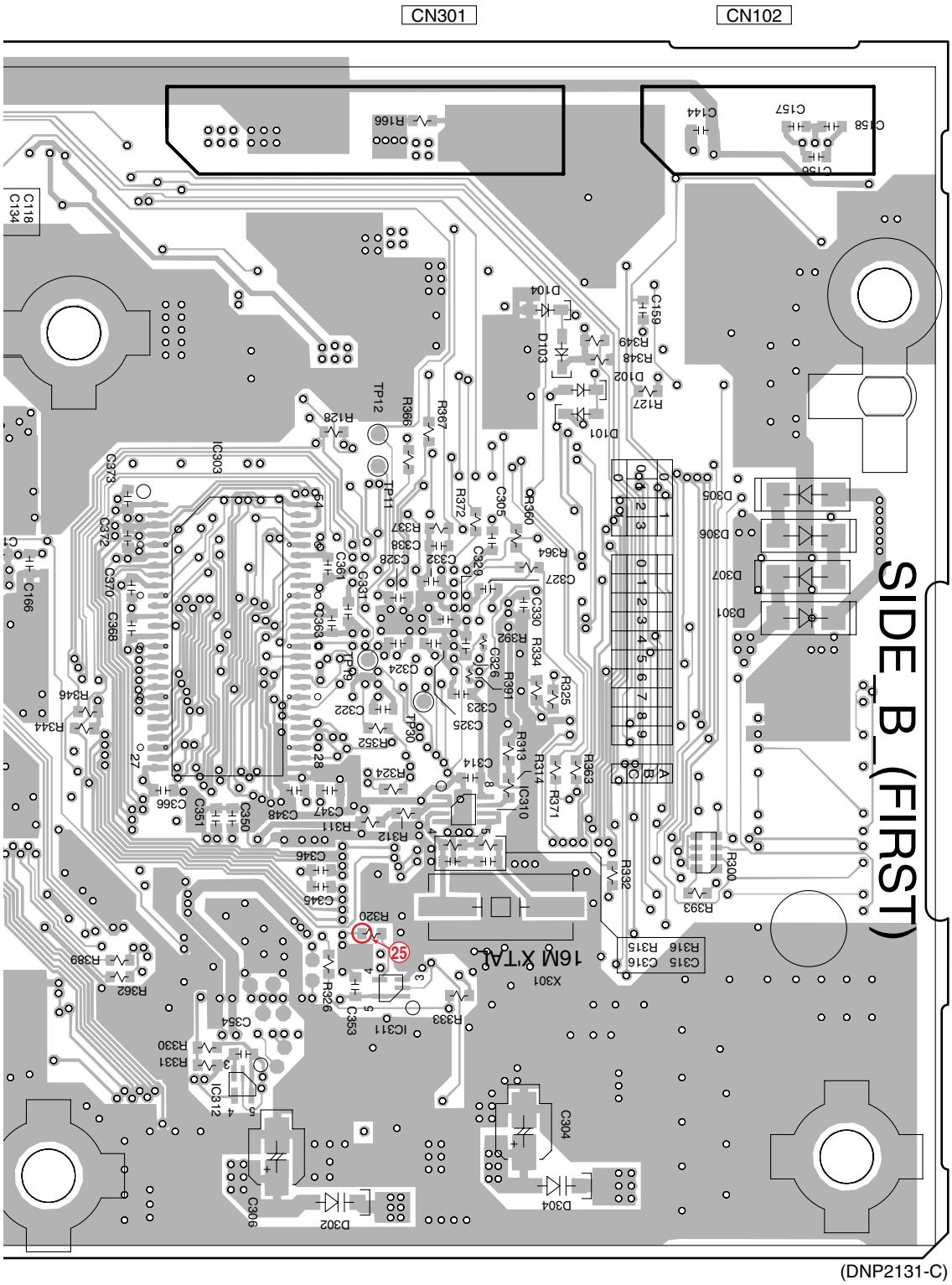
)0	Q101	IC105 IC703 IC106	IC702 IC704	IC100	
IC104	Q101	IC105 IC703 IC106	IC702 IC704	IC102	
)0	IC701			IC100	
IC104	IC701			IC102	

SIDE B

A MAIN ASSY



SIDE B



(DNP2131-C)

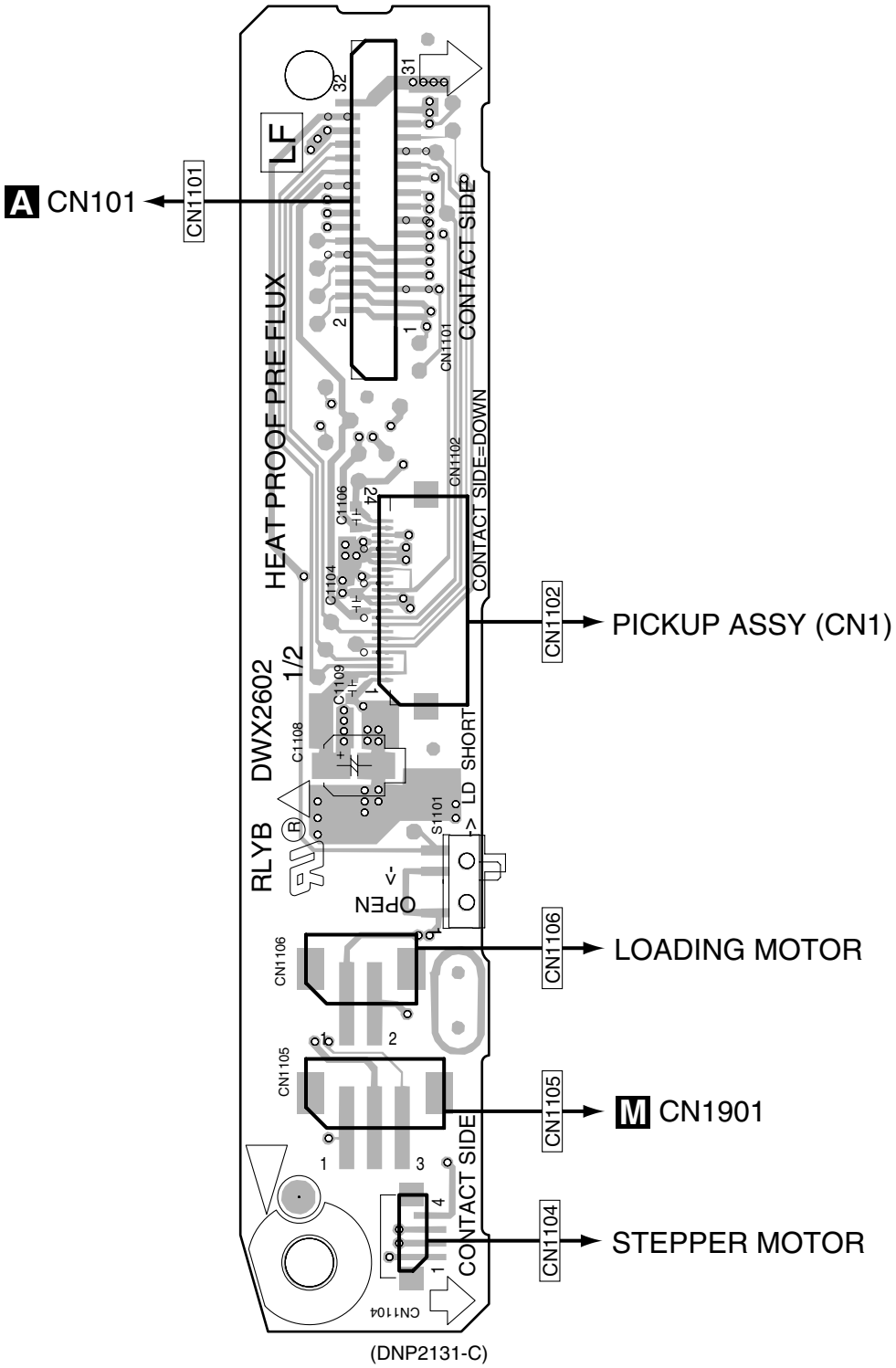
NOTE : The encircled numbers denote measuring point.

4.2 RLYB ASSY

SIDE A

SIDE A

B RLYB ASSY



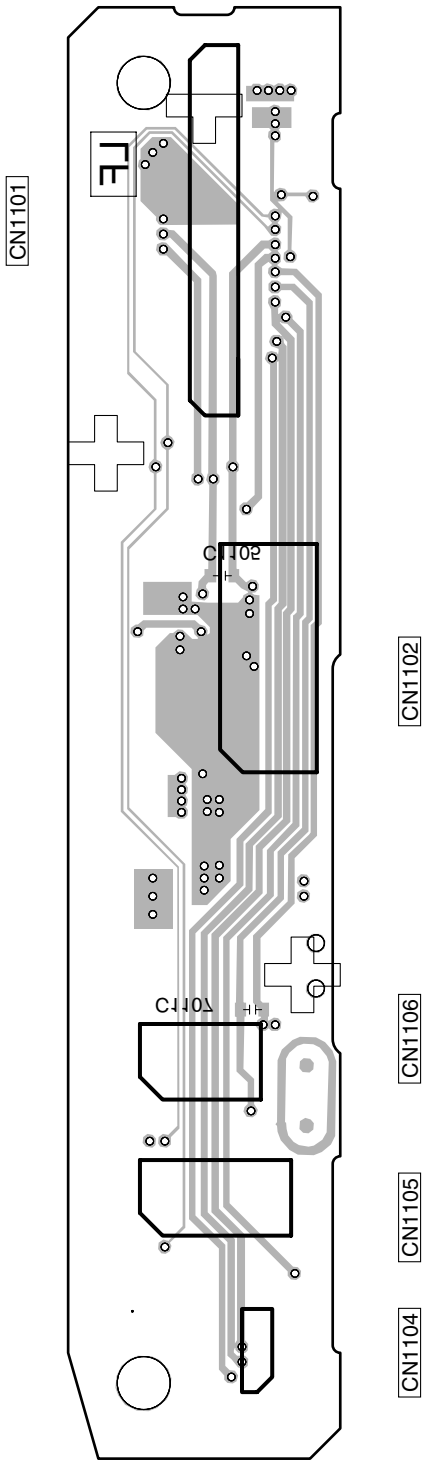
B

B

SIDE B

SIDE B

B RLYB ASSY

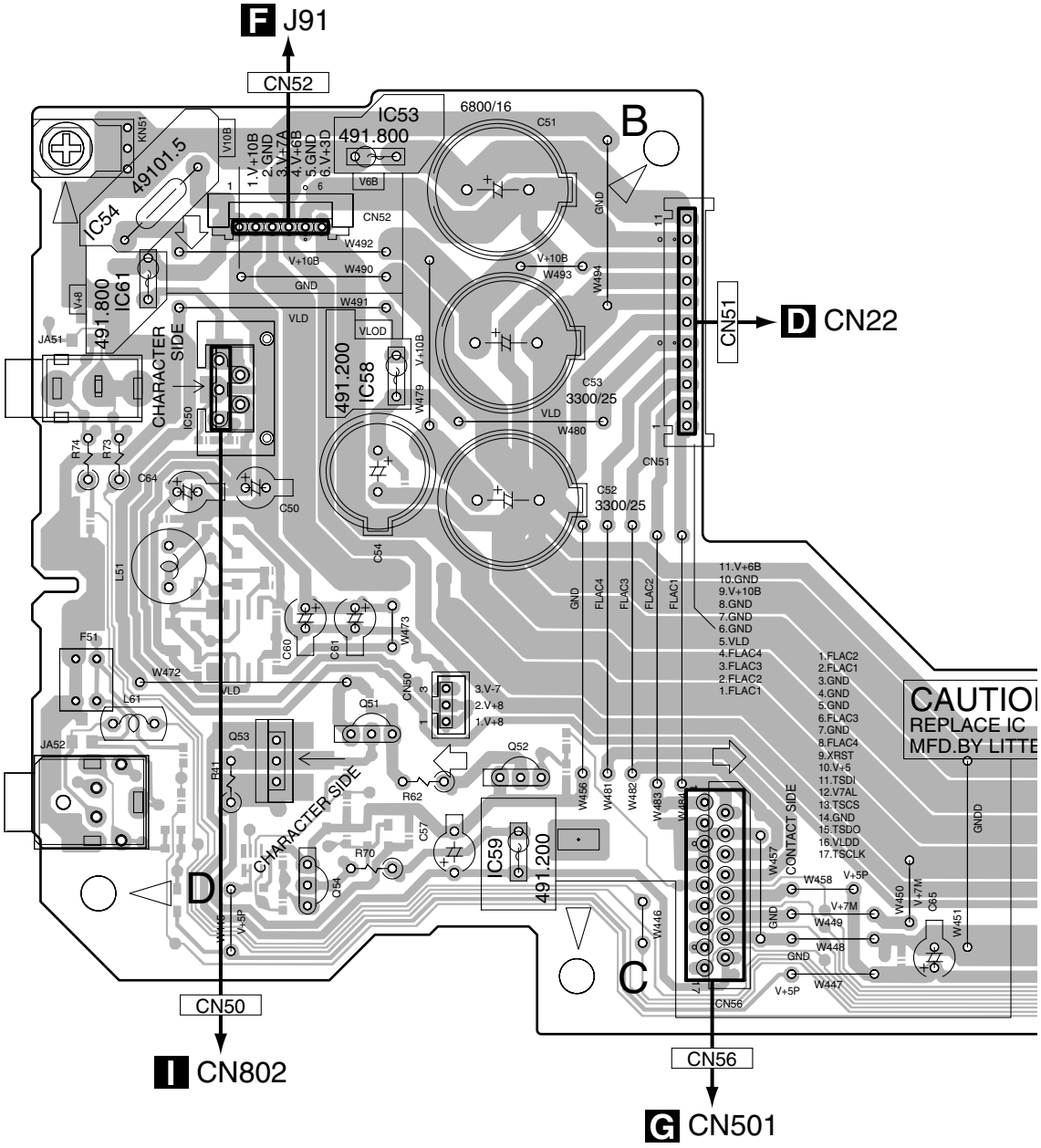


(DNP2131-C)

4.3 SECB ASSY

SIDE A

C SECB ASSY



SIDE A

A

B

IC53

IC54

IC61

C

IC58
IC50

D

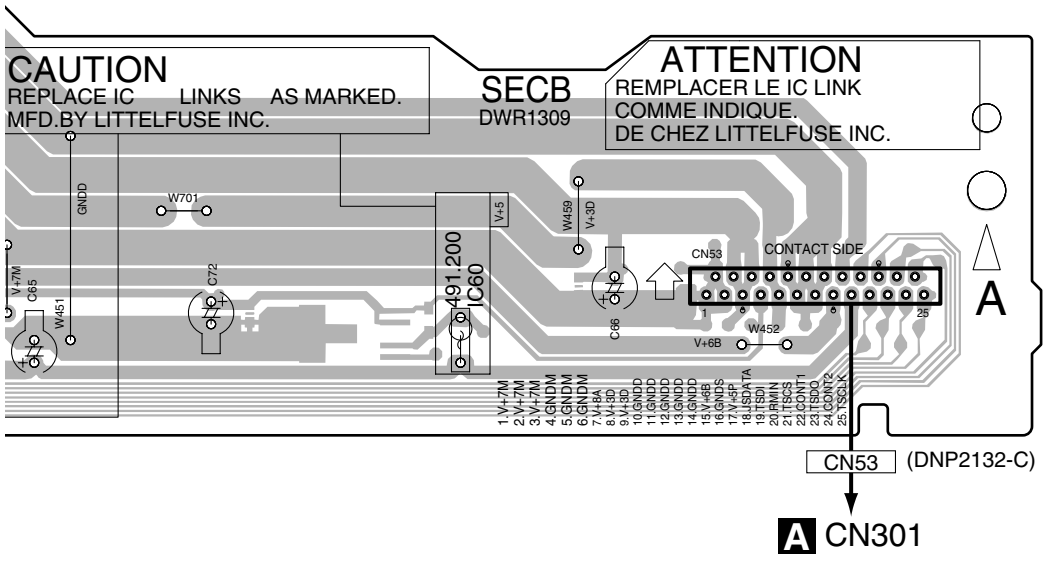
Q51

Q53 Q52

IC59 Q54

IC60

E



CN53 (DNP2132-C)

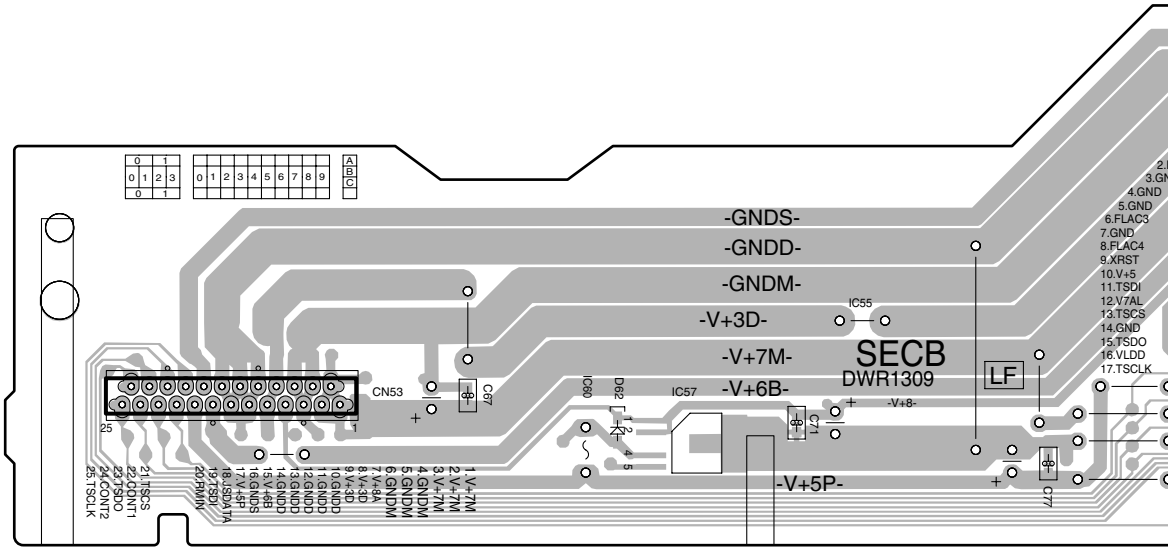
A CN301

F

C

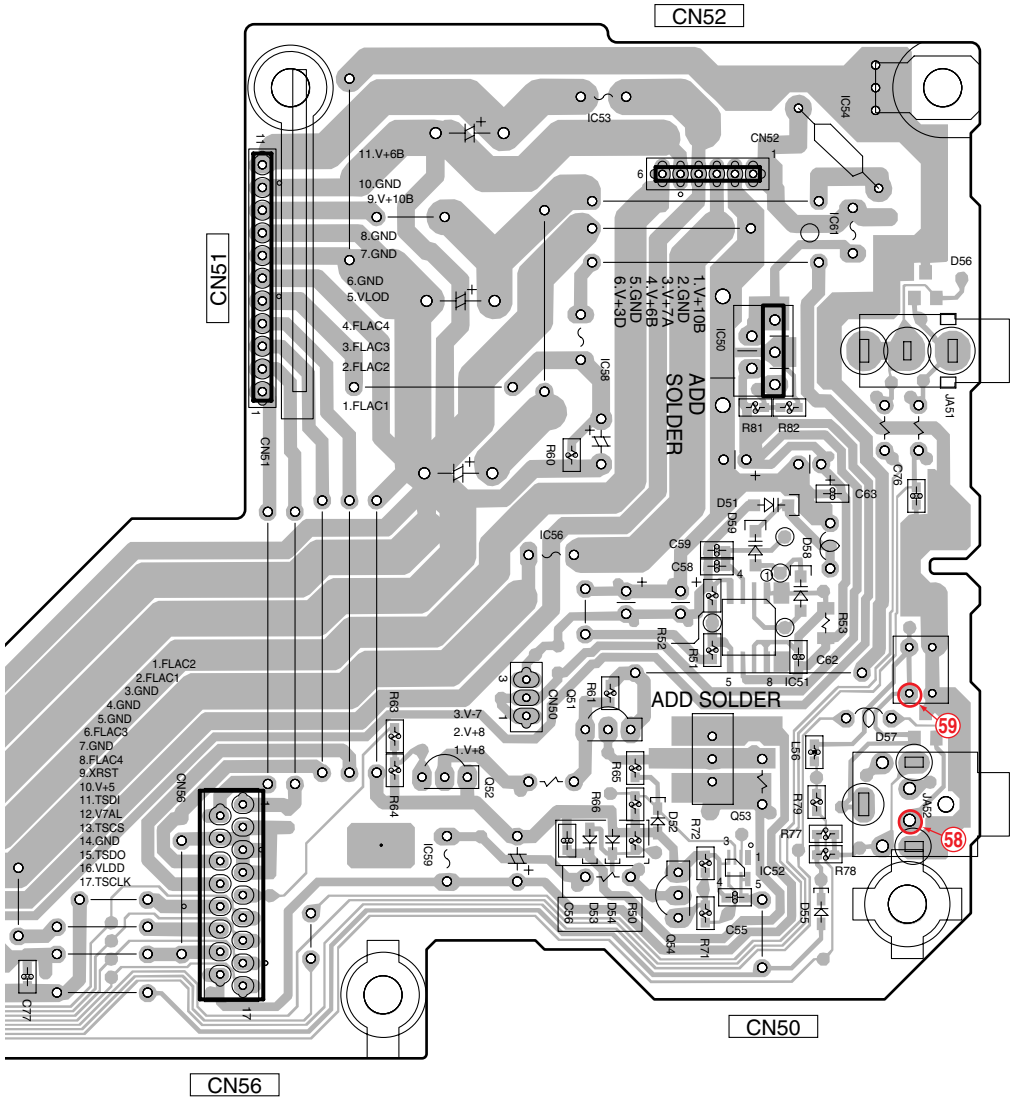
SIDE B

C SECB ASSY



(DNP2132-C) CN53

SIDE B



NOTE : The encircled numbers denote measuring point.

4.4 TRNS ASSY

SIDE A **SIDE A**

A

B

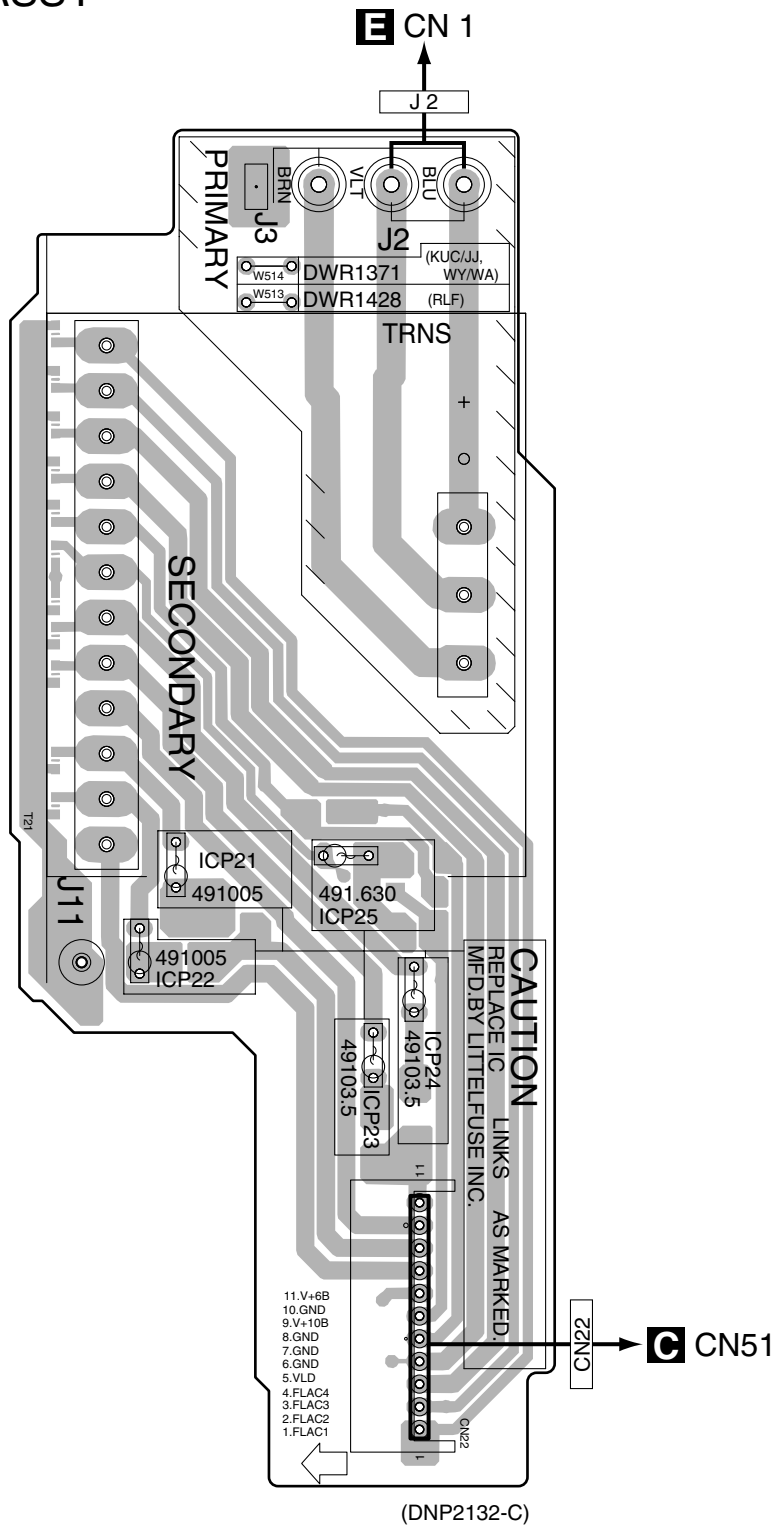
C

D

E

F

D TRNS ASSY



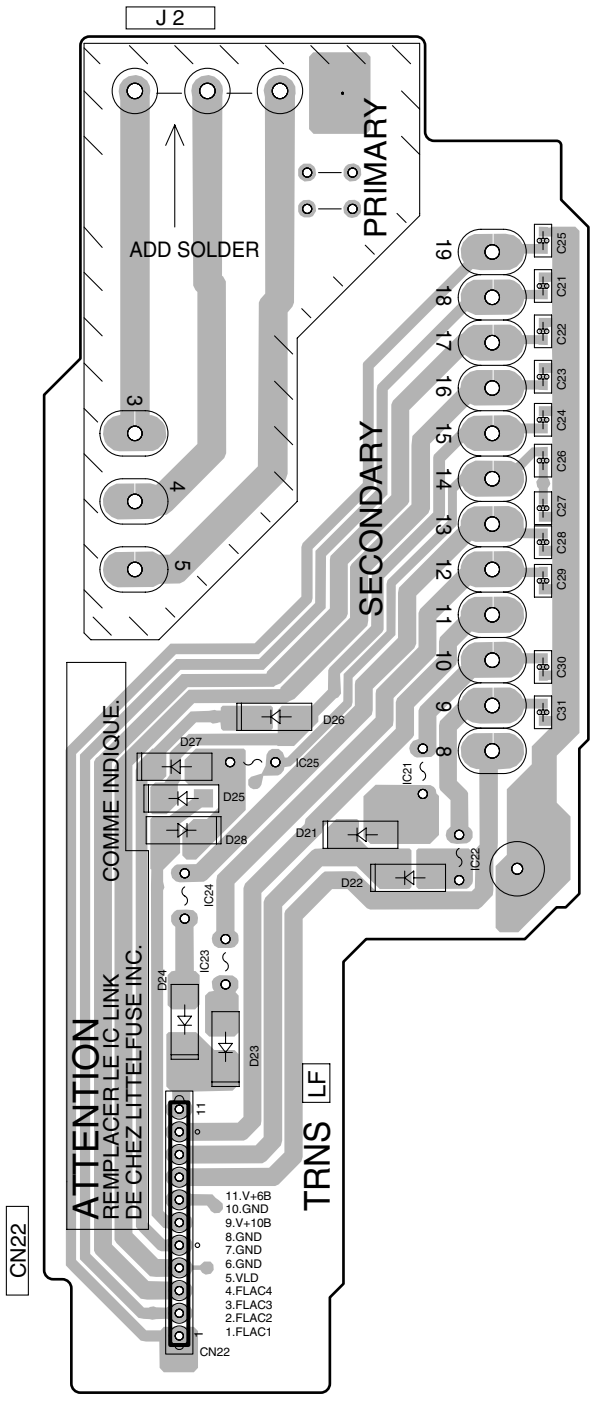
IC22 IC21 IC25 IC23 IC24

D **D**

SIDE B

SIDE B

D TRNS ASSY



(DNP2132-C)

IC24 IC23 IC25 IC21 IC22

4.5 AC IN ASSYS

SIDE A **SIDE A**

A

B

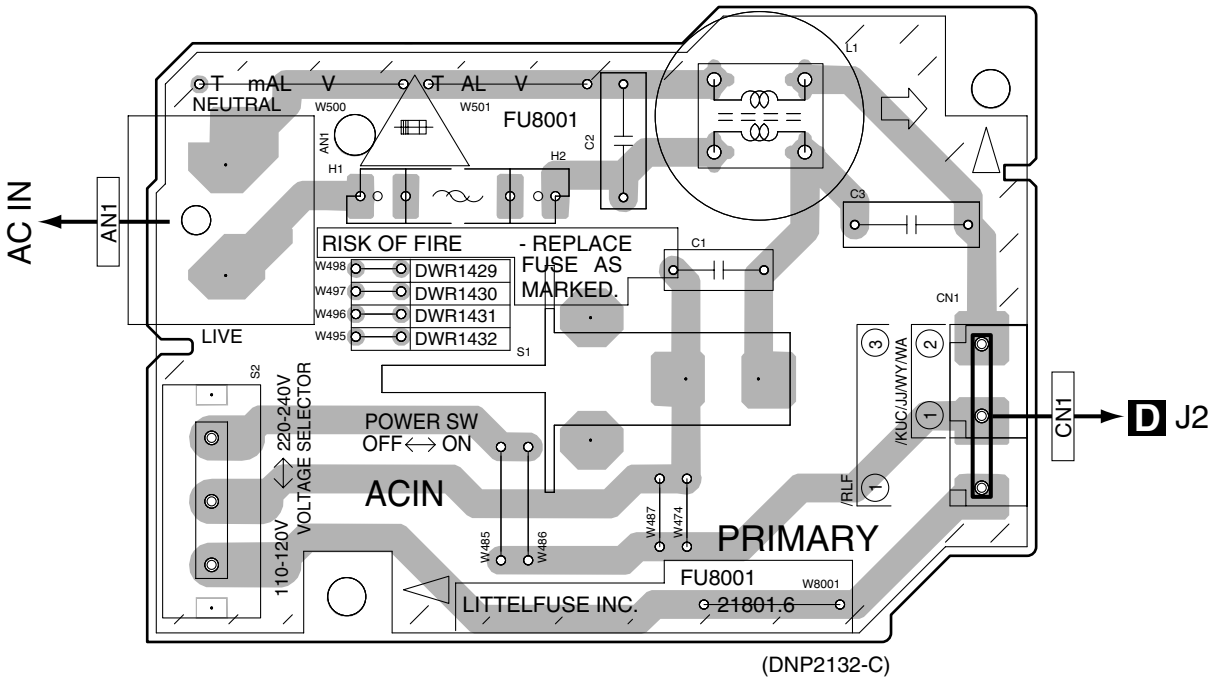
C

D

E

F

E ACIN ASSY



(DNP2132-C)

E **E**

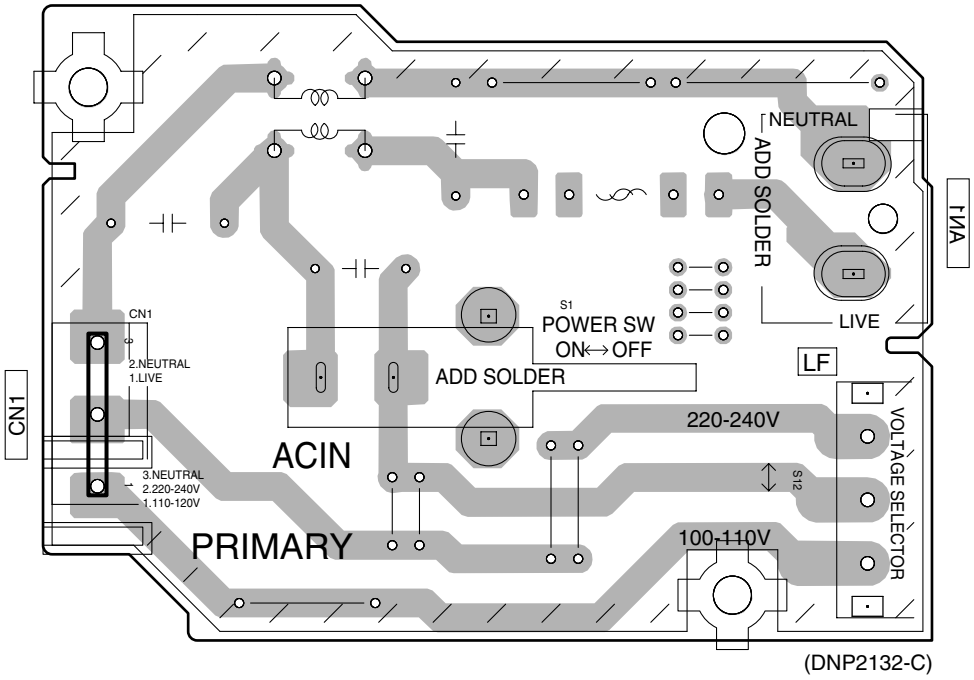
SIDE B

SIDE B

A

E ACIN ASSY

B



(DNP2132-C)

C

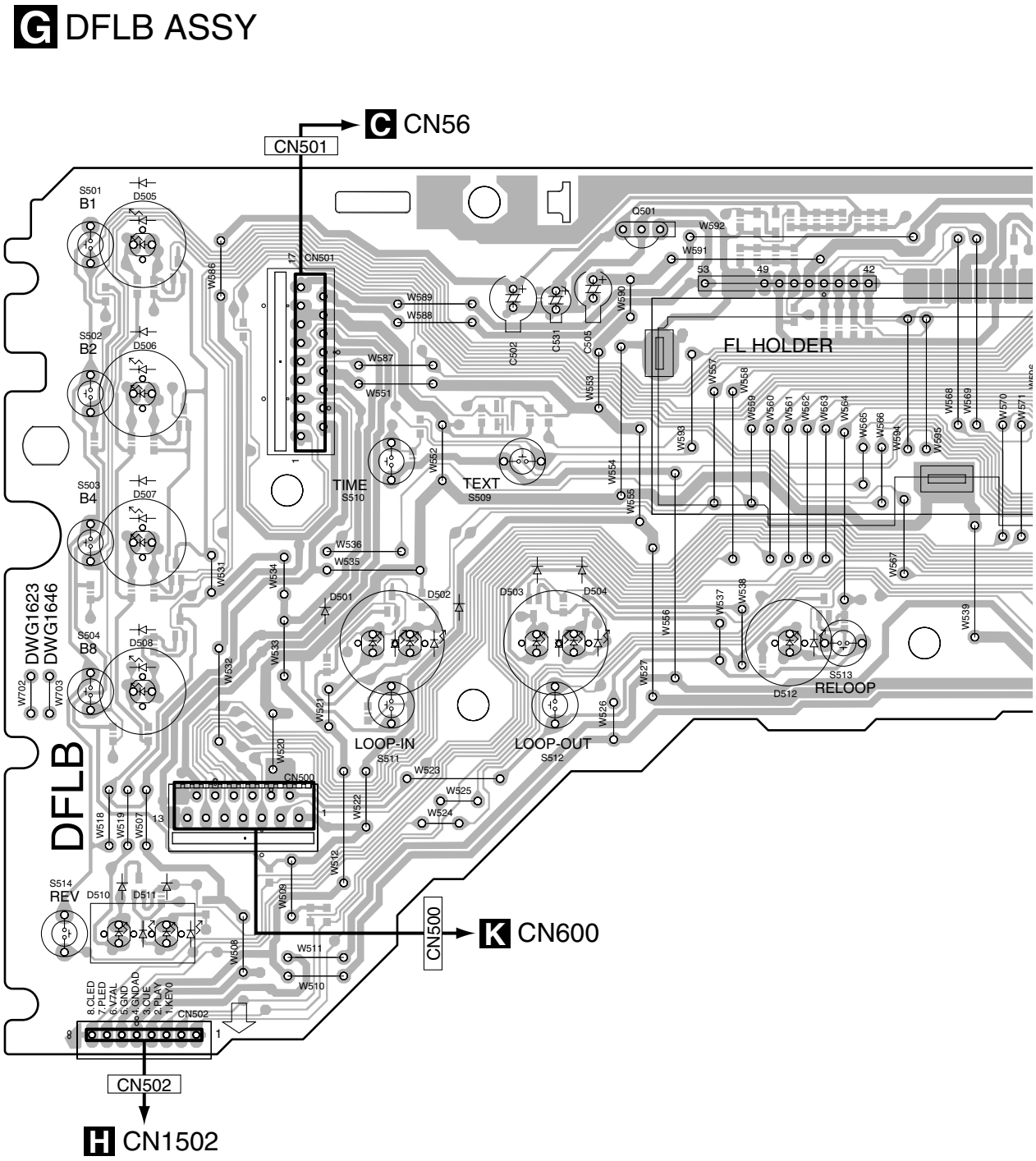
D

E

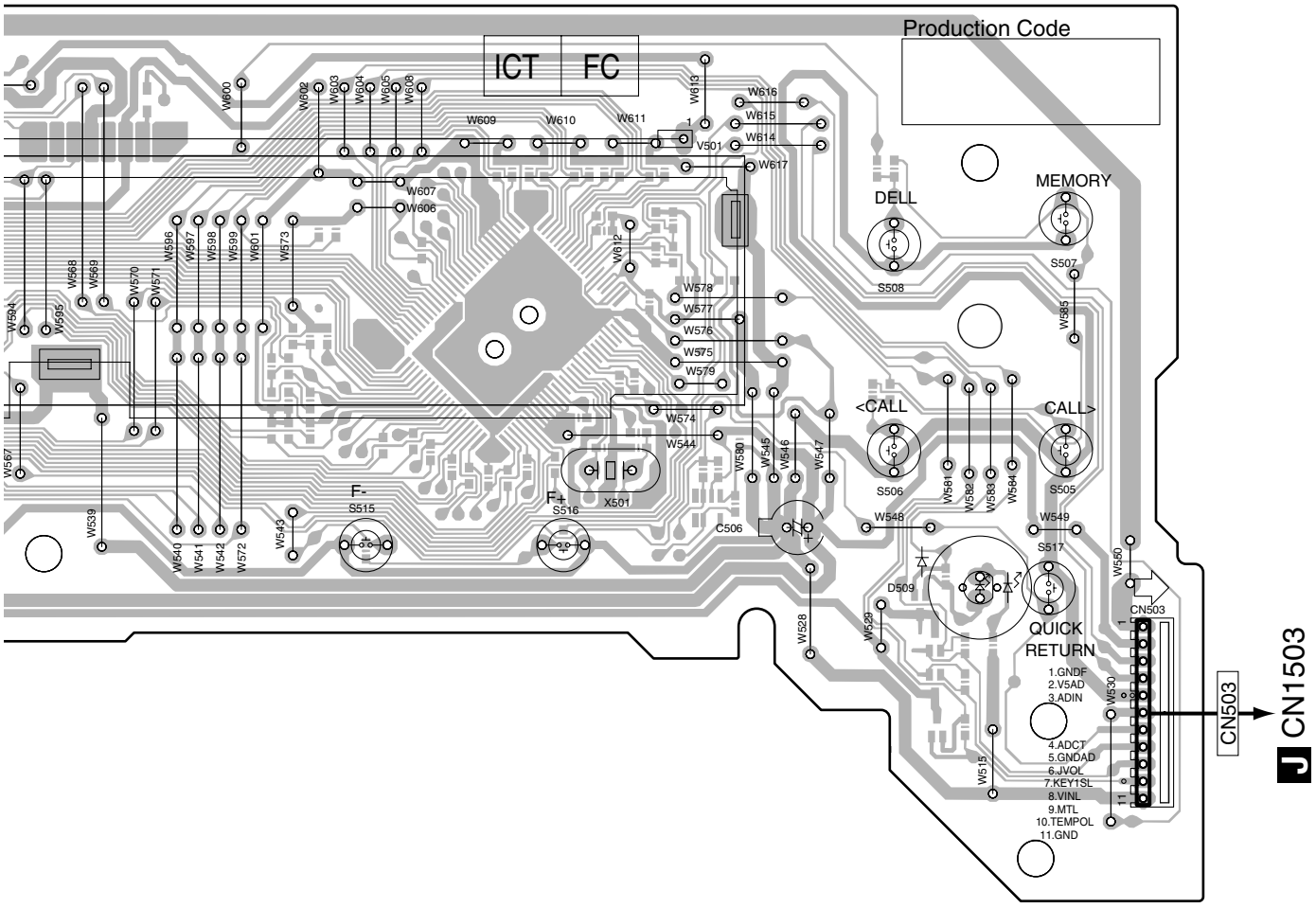
F

4.6 DFLB ASSY

SIDE A



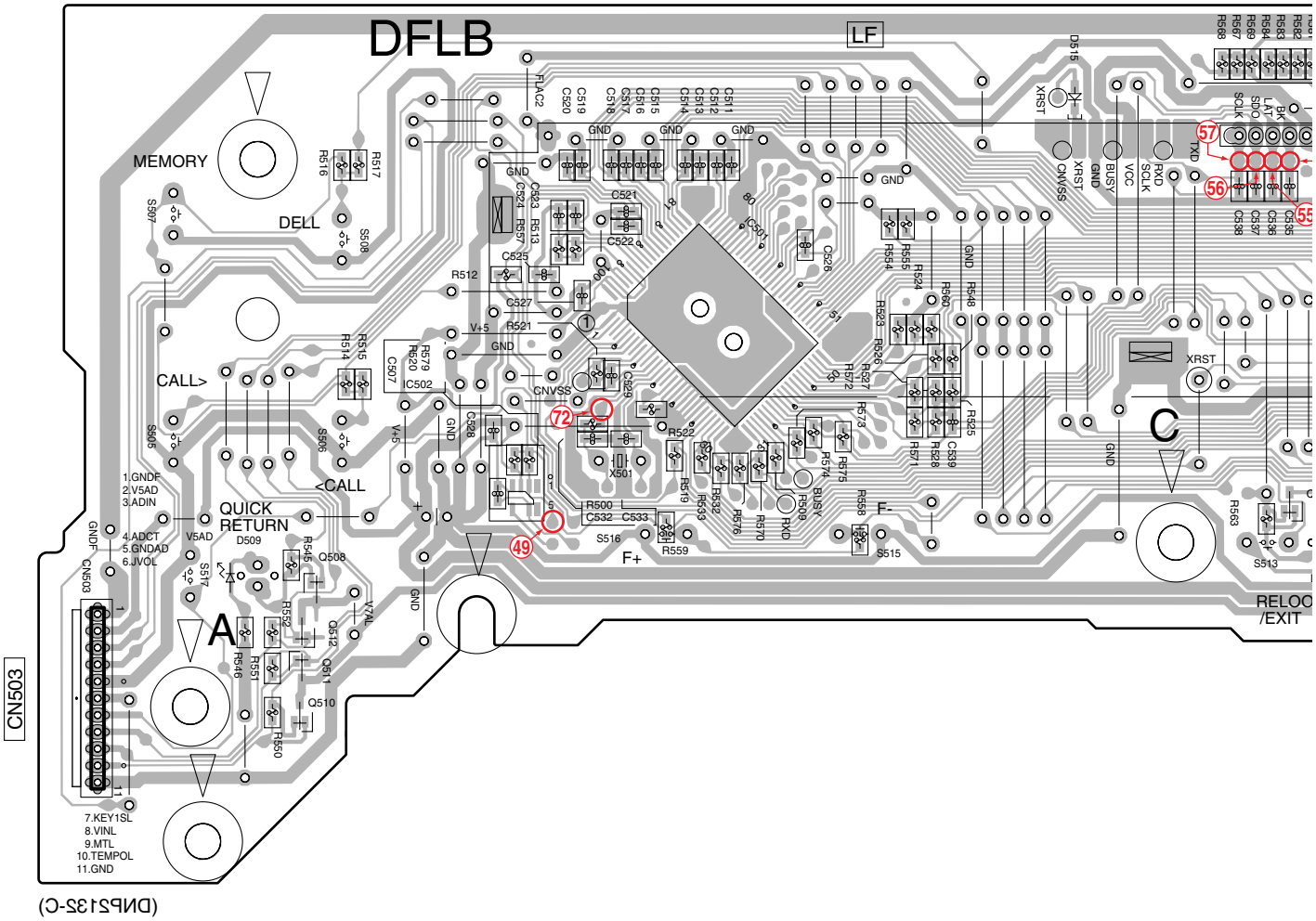
SIDE A



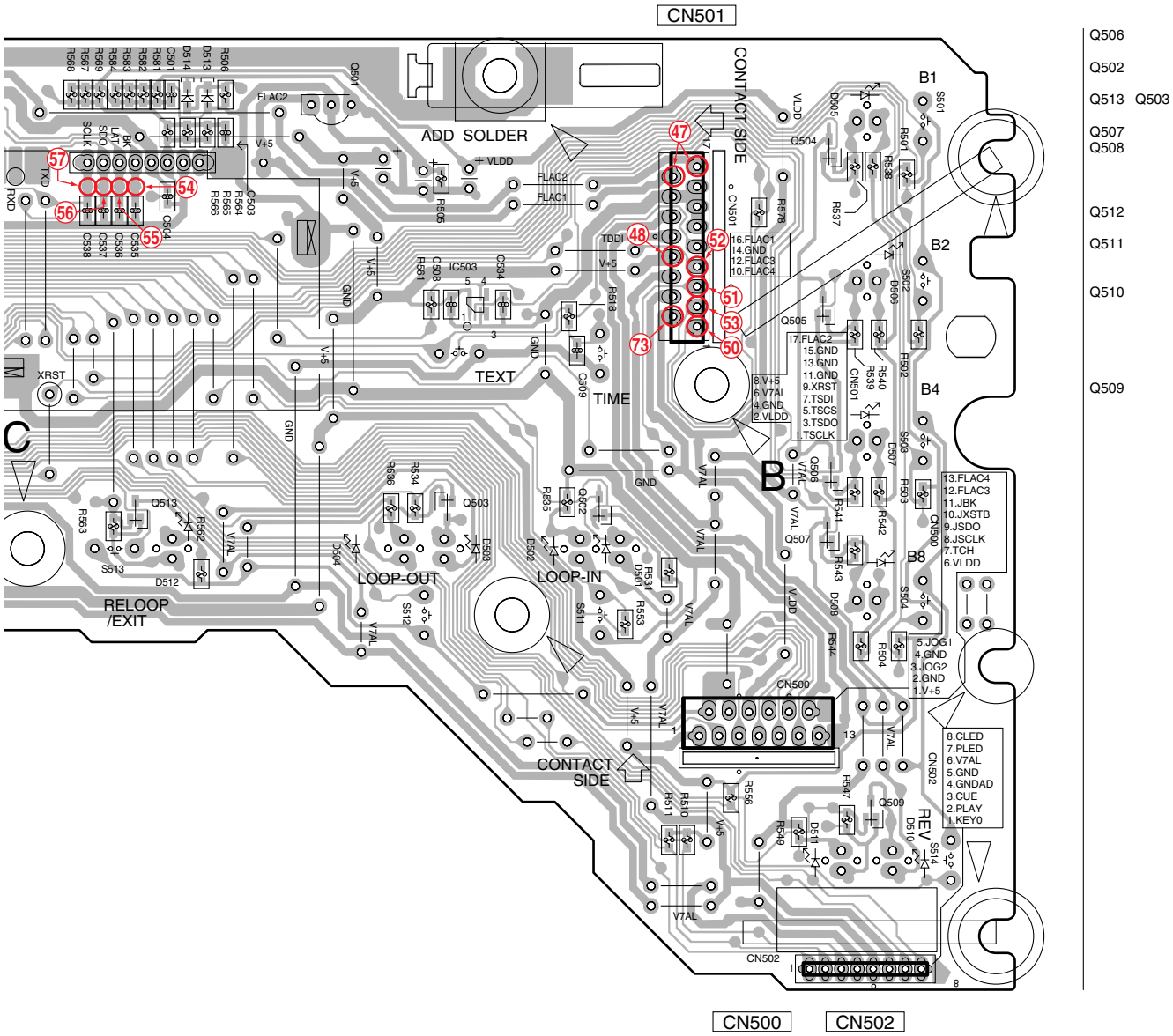
(DNP2132-C)

SIDE B

G DFLB ASSY



SIDE B



Q506
Q502
Q513 Q503
Q507
Q508
Q512
Q511
Q510
Q509

CN500 CN502

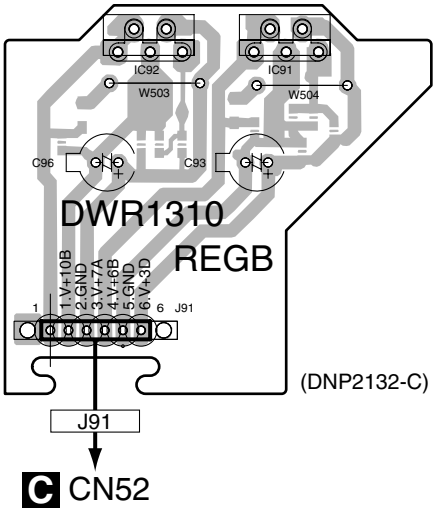
NOTE : The encircled numbers denote measuring point.

4.7 REGB and JACK ASSYS

SIDE A

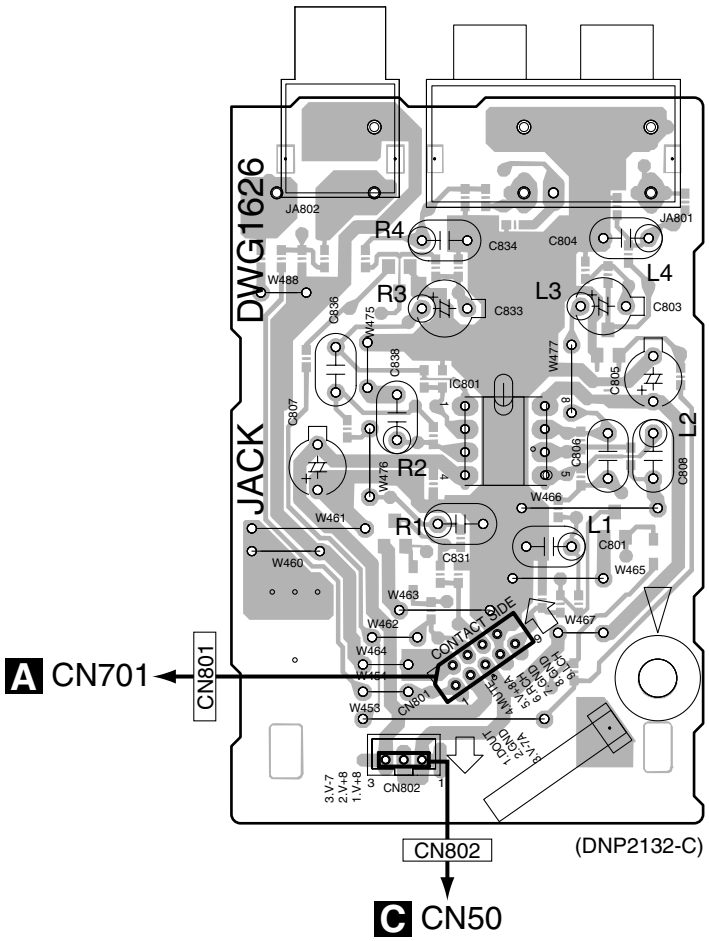
SIDE A

F REGB ASSY



IC92 IC91

I JACK ASSY



IC801

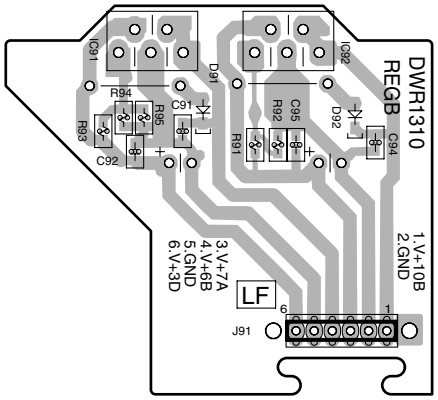
F **I**

F **I**

SIDE B

SIDE B

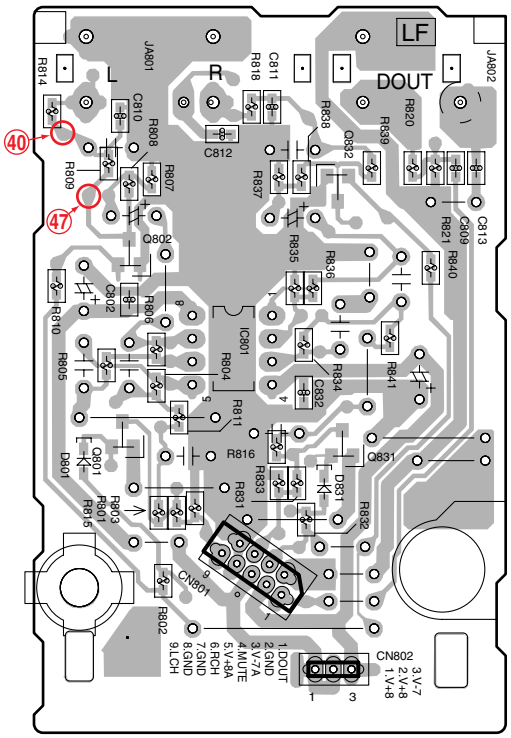
F REGB ASSY



(DNP2132-C)

J91

I JACK ASSY



CN801 CN802

(DNP2132-C)

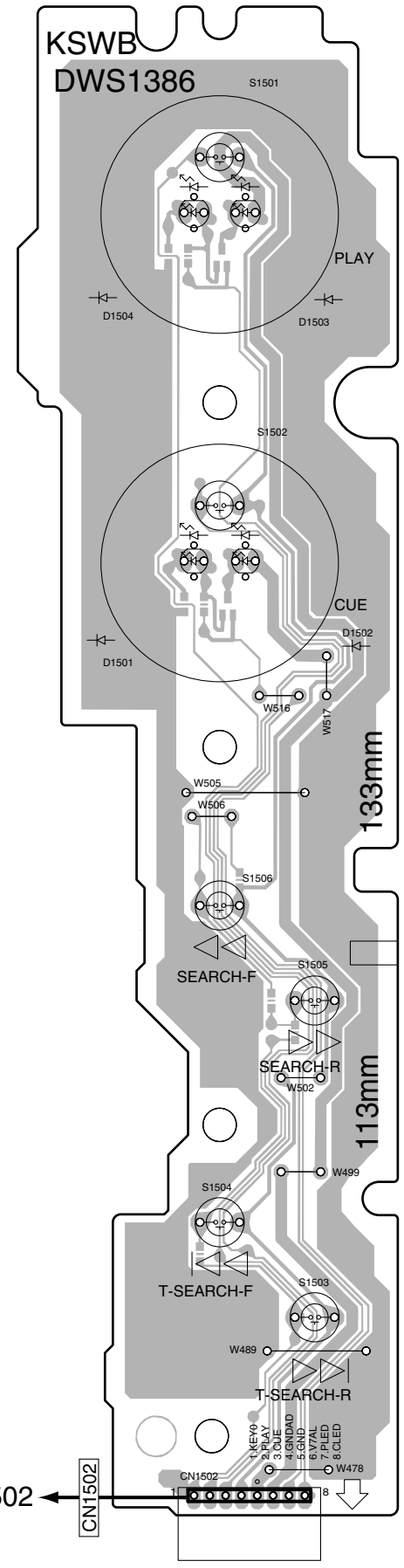
NOTE : The encircled numbers denote measuring point.

4.8 KSWB ASSY

SIDE A

SIDE A

H KSWB ASSY



G CN502

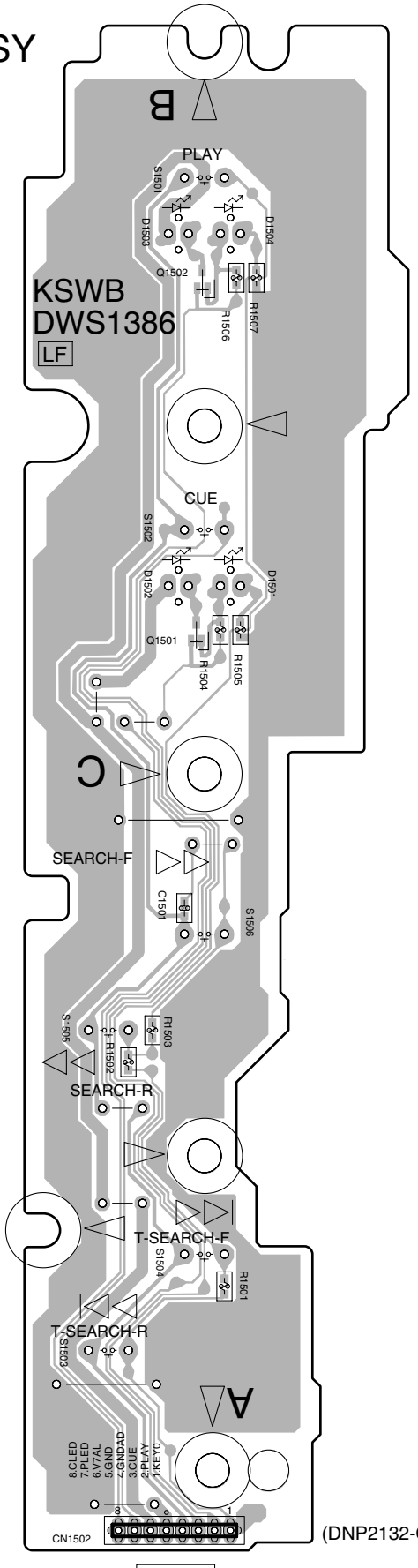
(DNP2132-C)

H

H

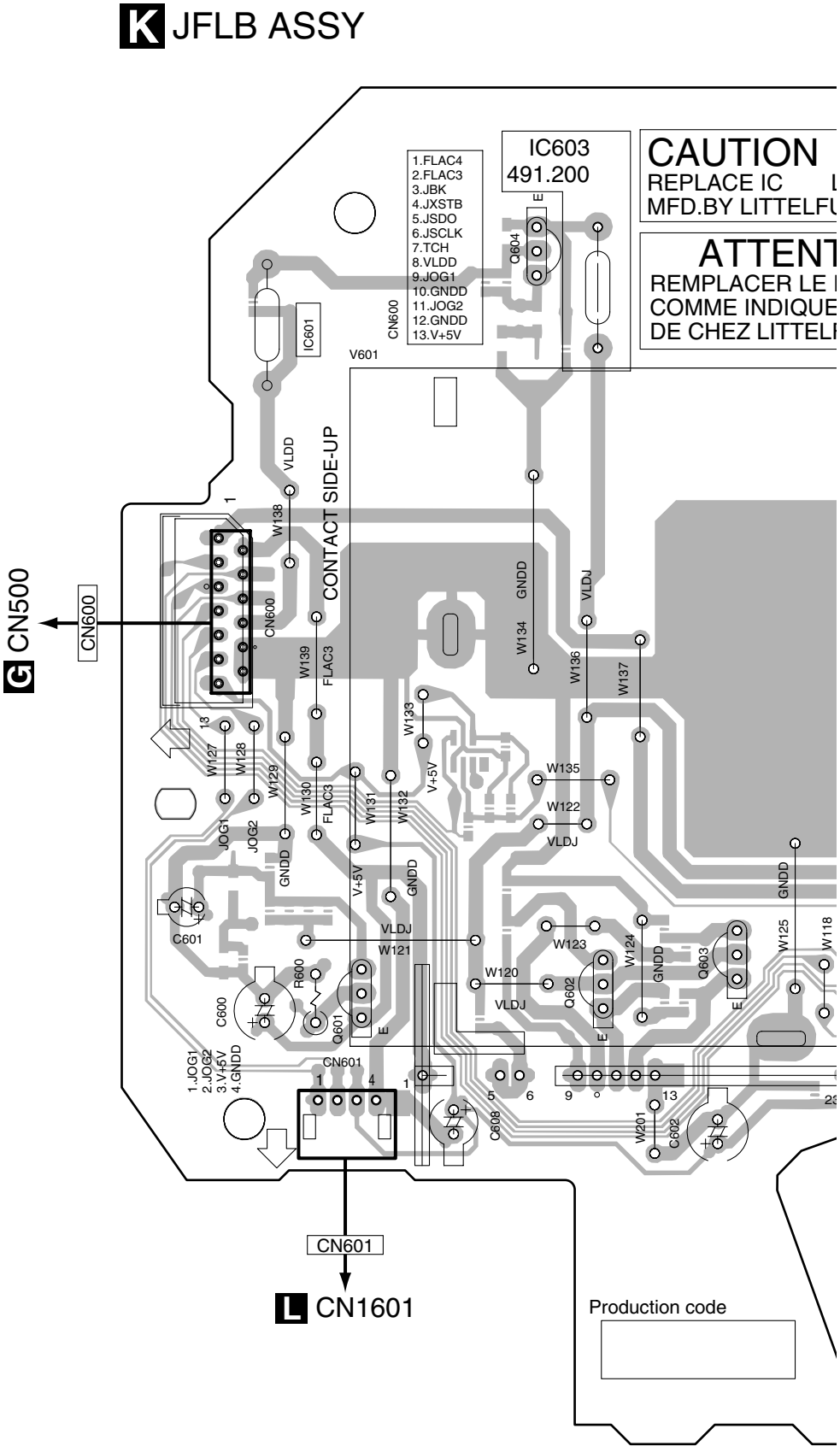
SIDE B **SIDE B**

H KSWB ASSY

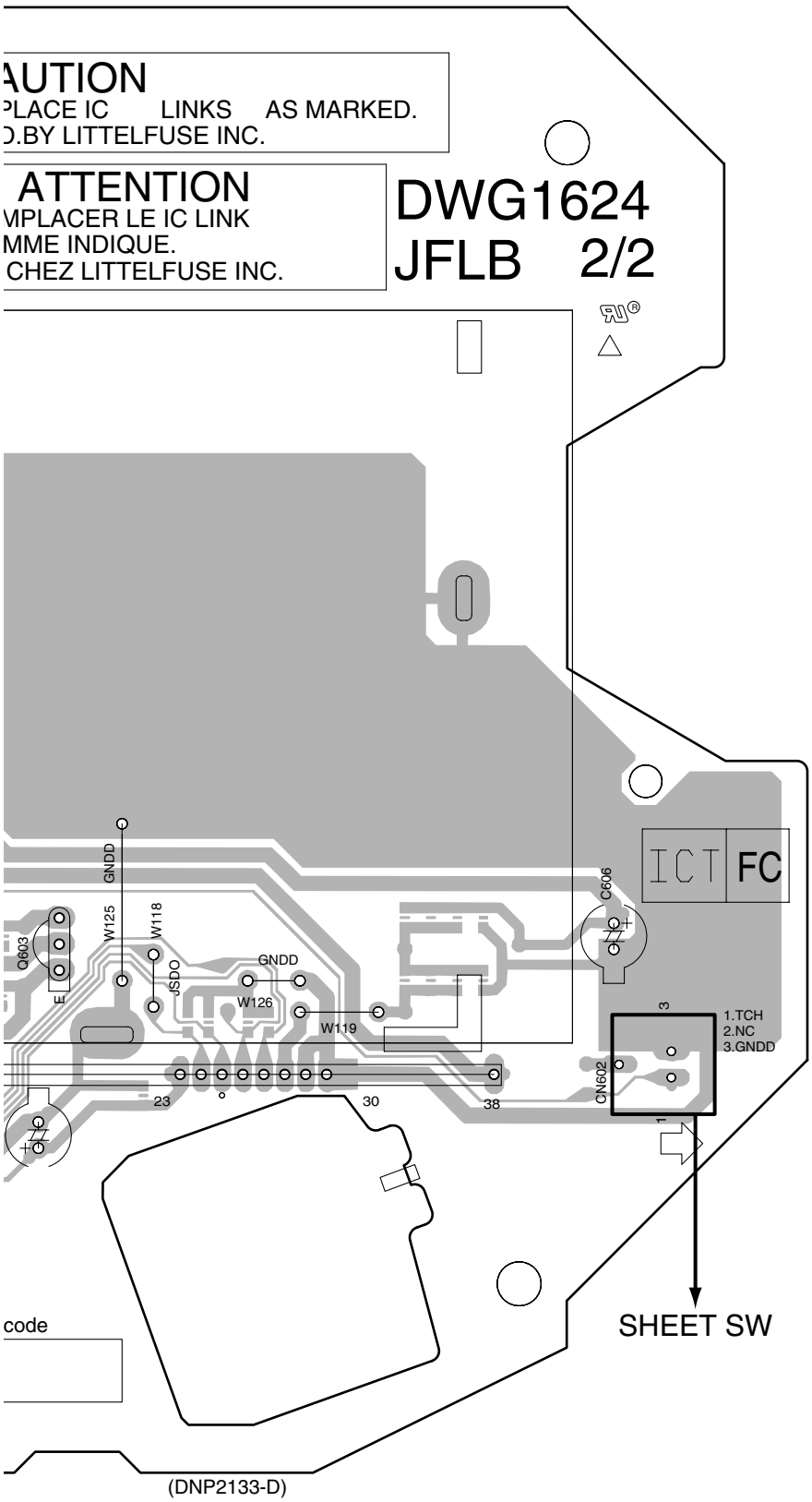


4.9 JFLB ASSY

SIDE A



SIDE A



IC603

Q604

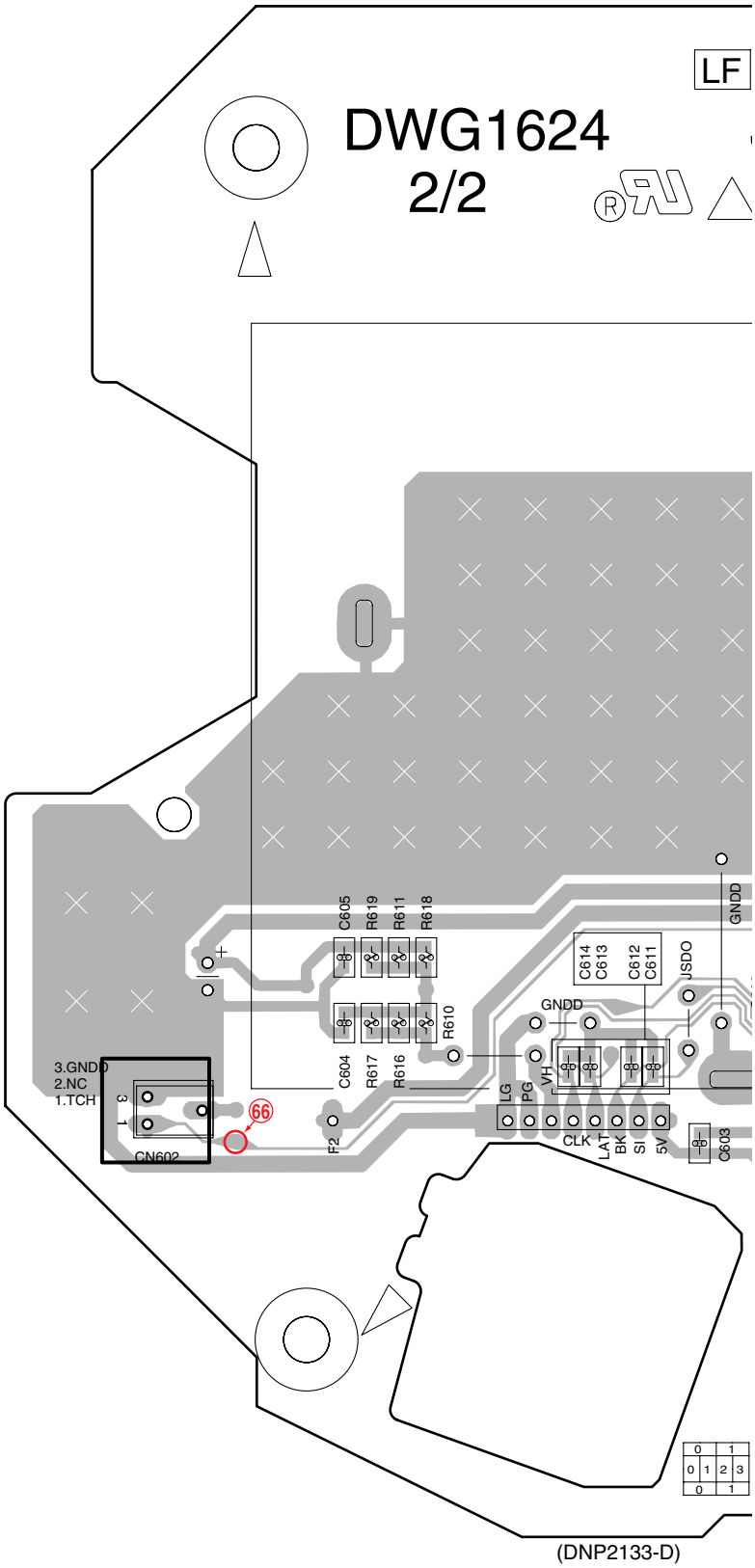
IC601

Q603
Q602
Q601

A B C D E F

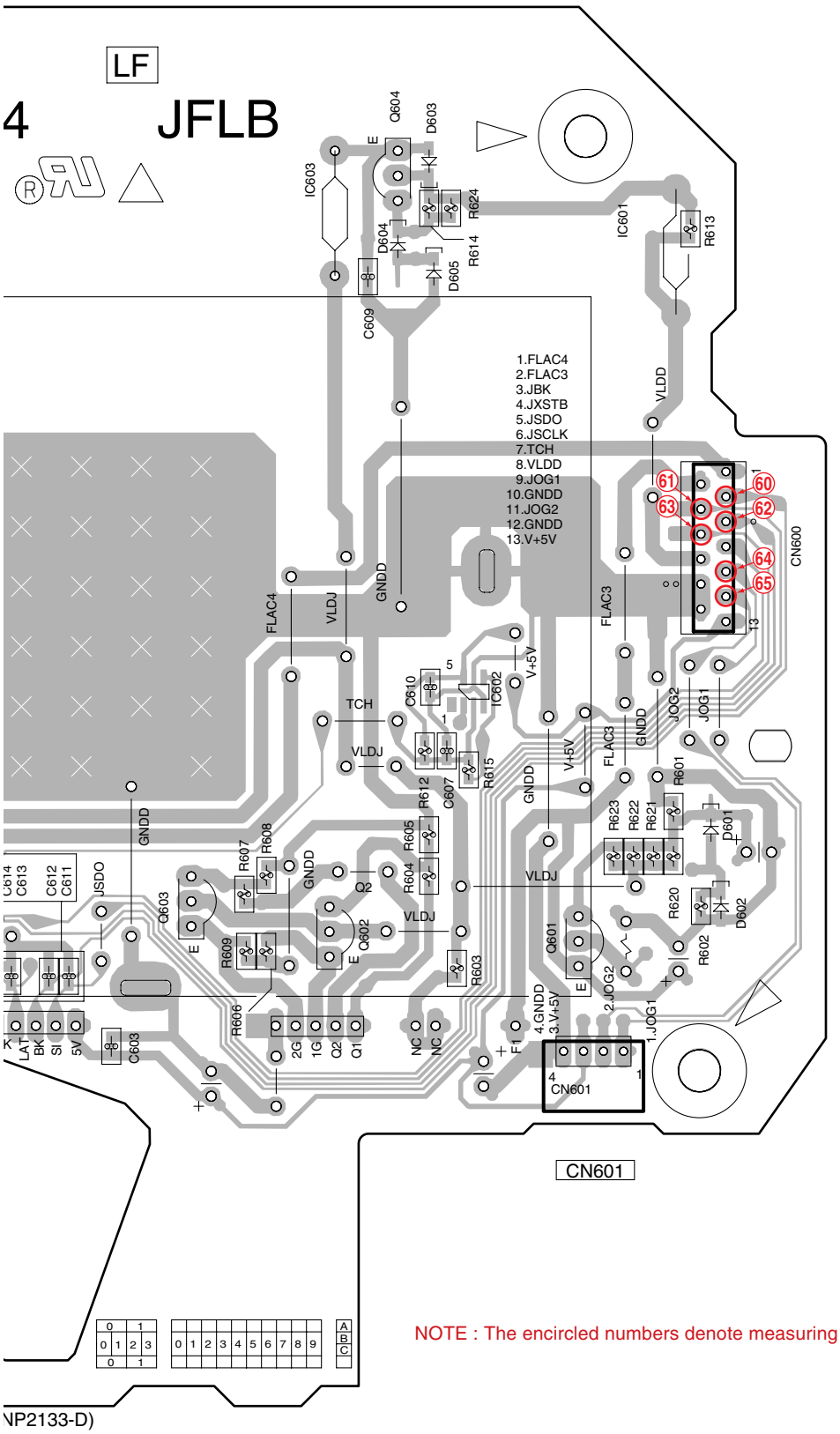
SIDE B

K JFLB ASSY



(DNP2133-D)

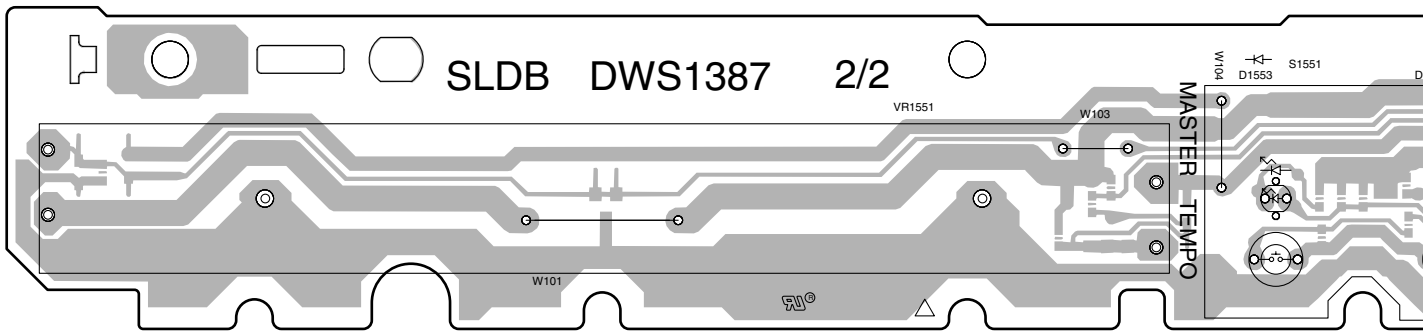
SIDE B


LF
4 JFLB
1.FLAC4
2.FLAC3
3.JBK
4.JXSTB
5.JSDO
6.JSCLK
7.TCH
8.VLDD
9.JOG1
10.GNDD
11.JOG2
12.GNDD
13.V+5V
CN600
CN601
IC602
NOTE : The encircled numbers denote measuring point.
NP2133-D)

4.10 SLDB ASSY

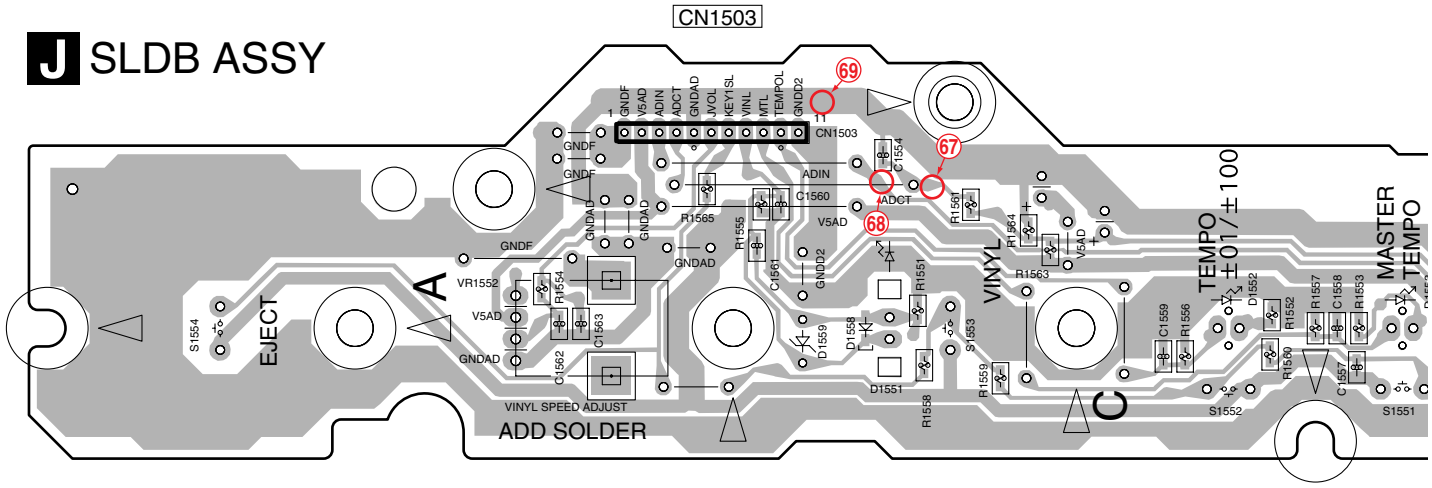
SIDE A

J SLDB ASSY

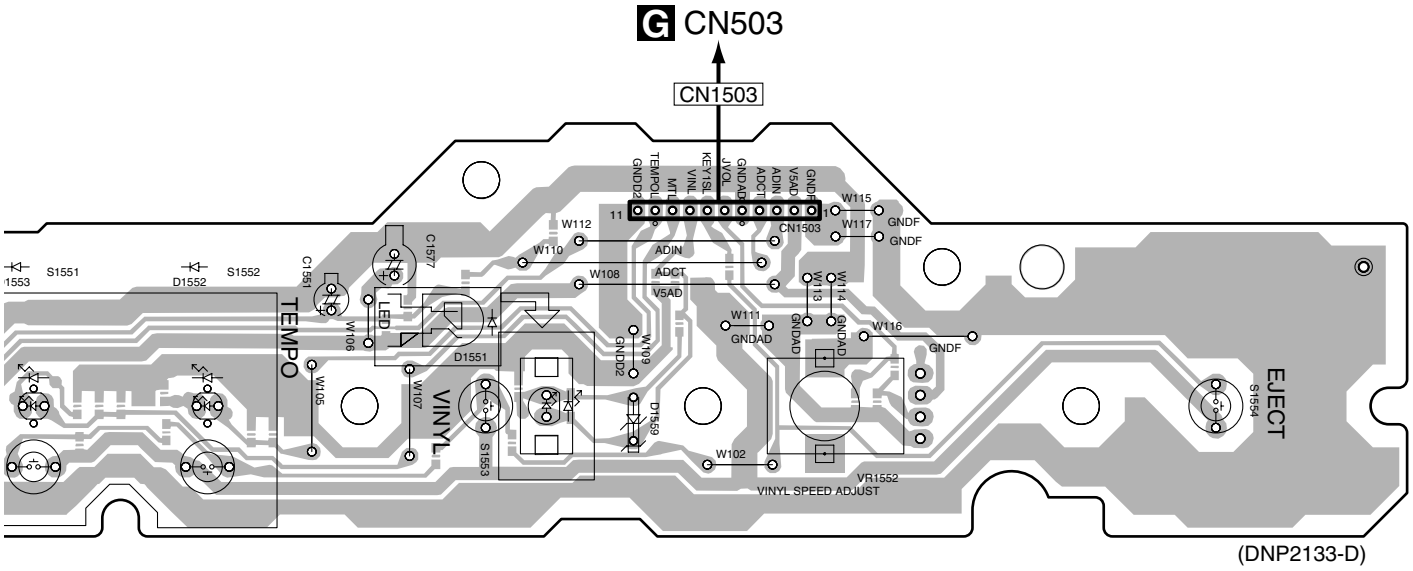


SIDE B

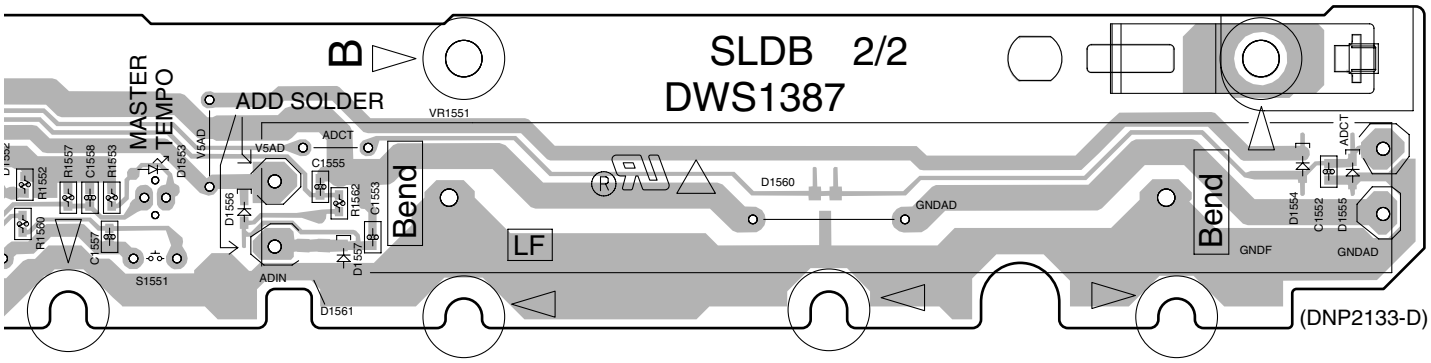
J SLDB ASSY



SIDE A



SIDE B



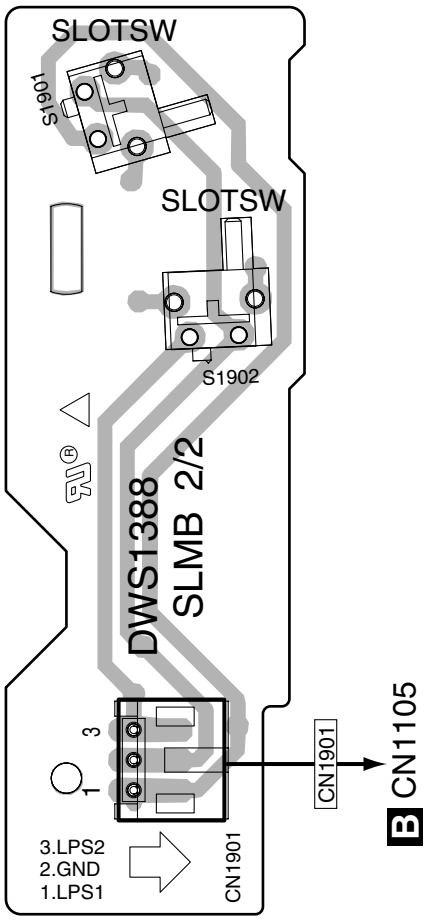
NOTE : The encircled numbers denote measuring point.

4.11 SLMB and JOGB ASSYS

SIDE A

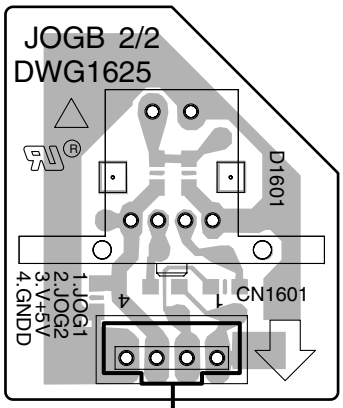
SIDE A

M SLMB ASSY



(DNP2133-D)

L JOGB ASSY



(DNP2133-D)

CN1601

K CN601

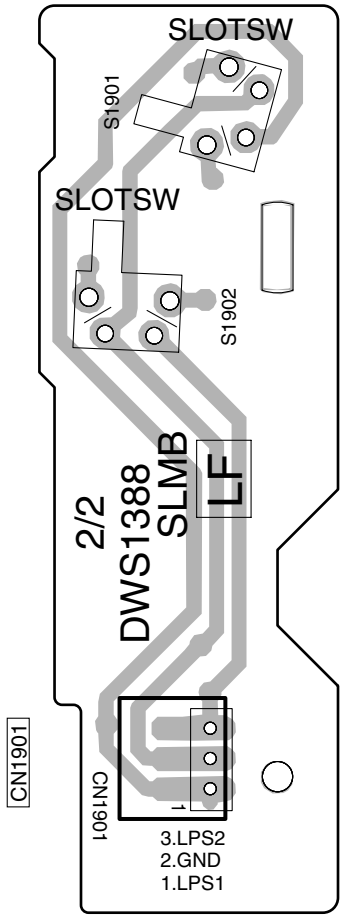
M L

M L

SIDE B

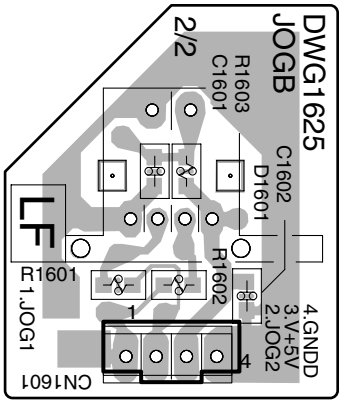
SIDE B

M SLMB ASSY



(DNP2133-D)

L JOGB ASSY



(DNP2133-D)

CN1601

5. PCB PARTS LIST

NOTES:
- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex.1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J=5%, and K=10%).

560 Ω → 56 x 10^1 → 561 ..... RD1/4PU 5 6 1 J
47k Ω → 47 x 10^3 → 473 ..... RD1/4PU 4 7 3 J
0.5 Ω → R50 ..... RN2H R 5 0 K
1 Ω → 1R0 ..... RS1P 1 R 0 K

Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).

5.62k Ω → 562 x 10^1 → 5621 ..... RN1/4PC 5 6 2 1 F

■ LIST OF HOLE PCB ASSEMBLIES

Mark	Symbol and Description	CDJ-800MK2/ KUCXJ	CDJ-200MK2/ WYXJ5	CDJ-800MK2/ RLFXJ
NSP	1..MOTHER ASSY	DWM2232	DWM2232	DWM2232
	2..MAIN ASSY	DWG1622	DWG1622	DWG1622
	2..RLYB ASSY	DWX2602	DWX2602	DWX2602
NSP	1..DISP ASSY	DWM2234	DWM2233	DWM2236
	2..DFLB ASSY	DWG1623	DWG1623	DWG1623
	2..JACK ASSY	DWG1626	DWG1626	DWG1626
	2..SECB ASSY	DWR1309	DWR1309	DWR1309
	2..REGB ASSY	DWR1310	DWR1310	DWR1310
	2..TRNS ASSY	DWR1371	DWR1371	DWR1428
	2..ACIN ASSY	DWR1430	DWR1429	DWR1432
	2..KSWB ASSY	DWS1386	DWS1386	DWS1386
NSP	1..SUB ASSY	DWM2237	DWM2237	DWM2237
	2..JFLB ASSY	DWG1624	DWG1624	DWG1624
	2..JOGB ASSY	DWG1625	DWG1625	DWG1625
	2..SLDB ASSY	DWS1387	DWS1387	DWS1387
	2..SLMB ASSY	DWS1388	DWS1388	DWS1388

■ CONTRAST OF PCB ASSEMBLIES

E ACIN ASSY

DWR1430, DWR1429 and DWR1432 are constructed the same except for the following :

Mark	Symbol and Description	DWR1430	DWR1429	DWR1432
⚠	AN1 1P AC INLET	XKP3042	XKP3041	XKP3041
⚠	CN1 2P VH CONNECTOR	B2P3-VH	B2P3-VH	B2P3-VH
⚠	CN1 3P VH CONNECTOR	Not used	Not used	B3P5-VH
⚠	S2 VOLTAGE SELECTOR	Not used	Not used	DSA1026

D TRNS ASSY

DWR1371 and DWR1428 are constructed the same except for the following :

Mark	Symbol and Description	DWR1371	DWR1428
⚠	J2 CONNECTOR ASSY	DKP3621	Not used
⚠	J3 CONNECTOR ASSY	Not used	DKP3720

■ PCB PARTS LIST FOR CDJ-800MK2 UNLESS OTHER WISE NOTED

Mark	No.	Description	Part No.

A MAIN ASSY

SEMICONDUCTORS

⚠	IC307, IC703	BD00KA5WFP
	IC304	BU4230G
	IC701	DSPC56371AF180
	IC300	DYW1753
	IC303	K4S641632K-UC75
	IC102	M63018FP
⚠	IC305	MM1561JF
⚠	IC306	MM1562FF
⚠	IC704	NJM2880U1-05
⚠	IC100	NJM2885DL1-33
	IC104	NJM2903M
	IC103	NJU7013F
	IC702	PE8001A
	IC301	SCF5249VM140
	IC308	TC74VHC08FTS1
	IC309	TC7SET08FUS1
	IC311, IC312	TC7SH08FUS1
	IC105	TC7W04FU
	IC106	TC7W08FU
	IC310	TC7WU04FU
	IC101	TC94A15FG
	IC302	XC3S50-4VQG100C
	Q101	2SA1036K
	Q707	2SC2412K
	Q302, Q303	2SC4081
	Q705	DTA124EUA
	Q304	DTA143EUA
	Q301, Q305, Q706	DTC124EUA
	D101–D104	1SS355

COILS AND FILTERS

	X301 (16.9 MHz)	VSS1084

CAPACITORS

	C160, C338	CCSRCH101J50
	C315, C316	CCSRCH150J50
	C146	CCSRCH221J50
	C142, C143	CCSRCH391J50
	C126, C153, C313, C317, C321	CCSRCH470J50
	C118, C337, C357	CCSRCH471J50
	C122, C154	CCSRCH680J50
	C135	CCSRCH681J50
	C100, C101, C700, C702	CEHVW101M10
	C105, C106, C301	CEHVW101M6R3
	C302, C304, C306, C712	CEHVW220M6R3
	C701, C703–C706	CEHVW470M16
	C102–C104	CEHVW470M6R3
	C132, C718	CKSRYB102K50
	C111, C129, C136, C141	CKSRYB103K50
	C156–C158, C165–C168, C303	CKSRYB103K50
	C305, C731–C734, C743	CKSRYB103K50
	C107–C110, C112–C117, C119	CKSRYB104K16
	C121, C124, C134, C137–C140	CKSRYB104K16
	C144, C149–C151, C159	CKSRYB104K16
	C161–C164, C307, C309, C312	CKSRYB104K16
	C314, C318, C319, C322–C335	CKSRYB104K16
	C339–C348, C350–C355	CKSRYB104K16
	C358, C359, C361, C363, C366	CKSRYB104K16
	C368, C370, C372, C373, C725	CKSRYB104K16
	C728–C730, C746–C758	CKSRYB104K16
	C145, C147, C148	CKSRYB105K10
	C320, C356, C360	CKSRYB105K6R3
	C152	CKSRYB152K50
	C120, C128	CKSRYB153K50
	C130, C131, C155	CKSRYB223K50
	C123, C127	CKSRYB333K25

RESISTORS

	R300, R747	RAB4C103J
	R154, R155, R170, R171	RS1/16S1002F
	R733	RS1/16S1801F
	R132, R133, R743	RS1/16S2202F
	R168, R321, R742	RS1/16S3302F
	R734	RS1/16S3901F
	R322	RS1/16S5602F
	R131	RS1/16S8201F
	R392	RS1/16SS000J
	Other Resistors	RS1/16S###J

OTHERS

	CN701 CONNECTOR	CKS4176
	CN102 CONNECTOR 13P	CKS4179
	CN301 CONNECTOR	CKS4192
	CN101 32P FFC CONNECTOR	DKN1447
	KN301 EARTH METAL FITTING	VNF1109

B RLYB ASSY

SWITCHES AND RELAYS

	S1101	VSH1018

CAPACITORS

	C1108	CEVW220M6R3
	C1105, C1107	CKSRYB103K50
	C1104, C1109	CKSRYB104K16

OTHERS

	CN1106 PH CONNECTOR 2P(SMT)	AKM1273
	CN1105 PH CONNECTOR 3P(SMT)	AKM1274
	CN1102 24P FFC CONNECTOR	DKN1445
	CN1101 32P FFC CONNECTOR	DKN1447
	CN1104 4P FFC CONNECTOR	VKN1409

C SECB ASSY

SEMICONDUCTORS

⚠	IC53, IC61	AEK7008
⚠	IC58–IC60	AEK7023
⚠	IC54	AEK7065
	IC50	BA00BC0WCP-V5
⚠	IC57	BA50BC0WFP
⚠	IC51	NJM2374AM
	IC52	TC7S04FU

Mark	No.	Description	Part No.
	Q51		2SB1238X
	Q52, Q54		2SD1859X
⚠	Q53		2SD2012
	D55		1SS355
	D51, D58, D59		EP05Q04
	D56, D57		NNCD6.2MF
	D53		UDZS30(B)
	D52		UDZS5R1(B)

COILS AND FILTERS

	L56	CTF1386
	L51	DTL1083
	L61	LRCA180J

CAPACITORS

	C59	CCSRCH181J50
	C58	CCSRCH220J50
	C50, C60, C64	CEHAT101M10
	C57	CEHAT1R0M50
	C54	CEHAT221M2A
	C61, C65, C66, C72	CEHAT330M25
	C56, C71	CKSRYB103K50
	C55, C63, C67, C76, C77	CKSRYB104K16
	C62	DCH1200
	C52, C53	DCH1223
	C51	DCH1224

RESISTORS

	R41	RD1/2VM102J
	R74	RD1/2VM271J
	R70	RD1/2VM330J
	R73	RD1/2VM471J
	R62	RD1/2VM562J
	R81	RS1/16S1203F
	R51, R82	RS1/16S2202F
	R52	RS1/16S4701F
	R53	RS1/4SA4R7J
	Other Resistors	RS1/16S###J

OTHERS

	CN52 6P JUMPER CONNECTOR	52147-0610
	JA52 MINI JACK	AKN7003
	CN50 FFC BOTTOM CONNECTOR	B3B-PH-K
	CN56 FFC CONNECTOR 17P	HLEM17S-1
	CN51 11P SOCKET	KP250NA11
	JA51 JACK	RKN1004
	PCB BINDER	VEF1040
	CN53 25P FFC CONNECTOR	VKN1256
	KN51 WRAPPING TERMINAL	VNF1084
	HEAT SINK	VNH1074

D TRNS ASSY (DWR1371)

SEMICONDUCTORS

⚠	IC25 (630 mA)	AEK7006
⚠	IC23, IC24 (3.5 A)	AEK7017
⚠	IC21, IC22 (5.0 A)	AEK7019
⚠	D25–D28	1SR154-400
⚠	D21–D24	RB060L-40
	C21–C31	CKSRYB473K50

OTHERS

⚠	J2	DKP3621
	CN22 11P CONNECTOR	S11B-XH-A-1
	PCB BINDER	VEF1040

D TRNS ASSY (DWR1428)

SEMICONDUCTORS

⚠	IC25	AEK7006
⚠	IC23, IC24	AEK7017
⚠	IC21, IC22	AEK7019
⚠	D25–D28	1SR154-400
⚠	D21–D24	RB060L-40

CAPACITORS

	C21–C31	CKSRYB473K50

OTHERS

⚠	J3 CONNECTOR ASSY	DKP3620
	CN22 11P CONNECTOR	S11B-XH-A-1
	PCB BINDER	VEF1040

E ACIN ASSY (DWR1429)

COILS AND FILTERS

⚠	L1	VTL-004

SWITCHES AND RELAYS

⚠	S1	RSA1001

CAPACITORS

⚠	C2, C3	ACE7027
⚠	C1	ACG7033

OTHERS

	H1, H2 FUSE CLIP	AKR1004
⚠	CN1 2P-VH CONNECTOR	B2P3-VH
⚠	AN1 AC INLET 1P	XKP3041

E ACIN ASSY (DWR1430)

COILS AND FILTERS

⚠	L1	VTL-004

SWITCHES AND RELAYS

⚠	S1	RSA1001

CAPACITORS

⚠	C2, C3	ACE7027
⚠	C1	ACG7033

OTHERS

	H1, H2 FUSE CLIP	AKR1004
⚠	CN1 2P-VH CONNECTOR	B2P3-VH
⚠	AN1 AS INLET 1P	XKP3042

Mark	No.	Description	Part No.
E		**ACIN ASSY (DWR1432)**	
		COILS AND FILTERS	
⚠	L1		VTL-004
		SWITCHES AND RELAYS	
⚠	S2		DSA1026
⚠	S1		RSA1001
		CAPACITORS	
⚠	C2, C3		ACE7027
⚠	C1		ACG7033
F		**REGB ASSY**	
		SEMICONDUCTORS	
⚠	IC91, IC92		BA00BC0WCP-V5
		CAPACITORS	
	C93, C96		CEHAR101M10
	C91, C92, C94, C95		CKSRYB103K50
		RESISTORS	
	R93		RS1/16S1002F
	R94, R95		RS1/16S1202F
	R91		RS1/16S3902F
	R92		RS1/16S8201F
		OTHERS	
		6P CABLE HOLDER	51048-0600
	J91	JUMPER WIRE	D20PDY0610E
		REGULATOR PLAT	DNH2707
G		**DFLB ASSY**	
		SEMICONDUCTORS	
	IC502		BU4242G
	IC501		PEG237B
	IC503		TC7SET08FUS1
	Q501		2SB1237X
	Q502–Q513		2SC4081
	D515		1SS355
	D510, D511		SLI-343URCW(RST)
	D501–D508, D512		SLI-343YCW(RST)
	D509		TLGE68TG(NP)
	D514		UDZS6R2(B)
		COILS AND FILTERS	
	X501	(16.0 MHz)	DSS1149
		SWITCHES AND RELAYS	
	S501–S504, S511–S514		DSG1079
	S505–S510, S515–S517		VSG1024
		CAPACITORS	
	C532, C533, C538		CCSRCH120J50
	C534		CCSRCH121J50
	C535–C537		CCSRCH330J50
	C531		CEHAR100M16
	C506		CEHAR101M10
	C502		CEHAR220M35
	C505		CEHAR330M10
	C511–C520, C523–C525		CKSRYB102K50
	C501, C507, C526–C529		CKSRYB103K50
	C504, C508		CKSRYB104K16
	C521, C522		CKSRYB105K6R3
	C503		CKSRYF104Z50
		RESISTORS	
	Other Resistors		RS1/16S###J
		OTHERS	
	CN500	FFC BOTTOM CONNECTOR	13P52492-1320
	CN501	FFC BOTTOM VONNEVTOR	17P52492-1720
	V501	VFD	DEL1059
		FL HOLDER	DNF1736
	CN502	8P SOCKET	KP200IB8L
	CN503	B TO B CONNECTOR 11P	VKN1363
H		**KSWB ASSY**	
		SEMICONDUCTORS	
	Q1501, Q1502		2SC4081
	D1501, D1502		SLI-343YCW(RST)
	D1503, D1504		TLGE68TG(NP)
		SWITCHES AND RELAYS	
	S1501, S1502		DSG1079
	S1503-S1506		VSG1024
		RESISTORS	
	Other Resistors		RS1/16S###J
		OTHERS	
	CN1502	8P PLUG	AKM7032
I		**JACK ASSY**	
		SEMICONDUCTORS	
	IC801		NJM4558DX
	Q801, Q802, Q831, Q832		2SD2114K
	D801, D831		1SS355
		CAPACITORS	
	C803, C805, C807, C833		CEHAT101M16
	C802, C809, C832		CKSRYB104K16
	C801, C804, C831, C834		CQMBA102J50
	C806, C808, C836, C838		CQMBA152J50
		RESISTORS	
	R806, R836		RN1/16SE1102D
	Other Resistors		RS1/16S###J

Mark	No.	Description	Part No.
		OTHERS	
	CN802	KR CONNECTOR 3P	B3B-PH-K
	JA801	2P JACK	DKB1053
	JA802	1P JACK	PKB1033
		PCB BINDER	VEF1040
	CN801	9P FFC CONNECTOR	VKN1240

J SLDB ASSY

		SEMICONDUCTORS	
	D1554–D1557		1SS355
	D1551		E1L4E-9B1A(PQ)
	D1553		SLI-343URCW(RST)
	D1552		SLI-343YCW(RST)
		SWITCHES AND RELAYS	
	S1551–S1554		VSG1024
		CAPACITORS	
	C1551		CEHAR100M16
	C1552, C1553		CKSRYB102K50
	C1558–C1561		CKSRYB103K50
		RESISTORS	
	R1563, R1564		RS1/16S2201F
	VR1552		DCS1062
	VR1551		DCV1009
	Other Resistors		RS1/16S###J
		OTHERS	
	CN1503	B–B CONNECTOR	DKN1289

K JFLB ASSY

		SEMICONDUCTORS	
⚠	IC603		AEK7057
	Q601		2SB1237X
	Q602, Q603		2SC1815
	Q604		2SD1858X
	D603		1SS355
	D604		UDZS13(B)
	D605		UDZS15(B)
	D601		UDZS8R2(B)
		CAPACITORS	
	C611–C614		CCSRCH221J50
	C601		CEHAR100M16
	C600, C602		CEHAR101M10
	C606		CEHAR220M35
	C608		CEHAR330M10
	C607		CKSRYB102K50
	C603, C605, C609		CKSRYB103K50
	C604		CKSRYF104Z50
		RESISTORS	
	R600		RD1/2VM680J
	Other Resistors		RS1/16S###J

Mark	No.	Description	Part No.
		OTHERS	
	CN602	CONNECTOR	CKS1072
	V601	FL INDICATOR	DEL1058
		FL HOLDER	DNF1735
	CN600	FFC CONNECTOR 13P	HLEM13R-1
	CN601	KR CONNECTOR	S4B-PH-K

L JOGB ASSY

		SEMICONDUCTORS	
	D1601		GP1A038RBK
		CAPACITORS	
	C1601, C1602		CKSRYB103K50
		RESISTORS	
	Other Resistors		RS1/16S###J
		OTHERS	
	CN1601	KR CONNECTOR	B4B-PH-K

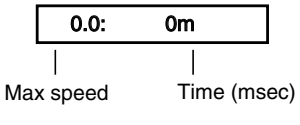
M SLMB ASSY

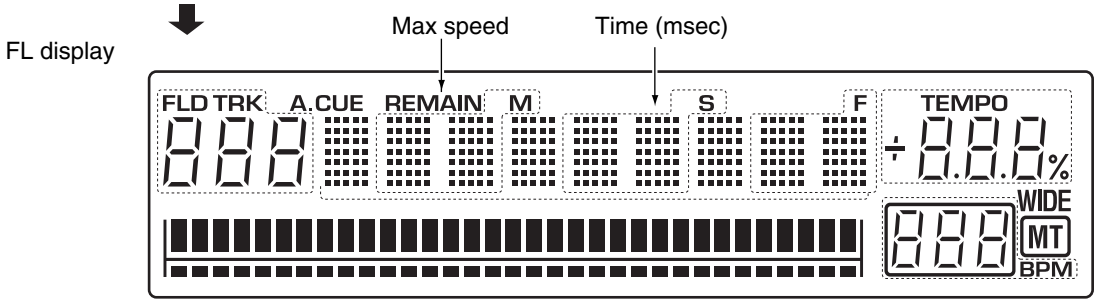
		SWITCHES AND RELAYS	
	S1901, S1902		DSG1017
		OTHERS	
	CN1901	KR CONNECTOR	S3B-PH-K

6. ADJUSTMENT

• Mode for checking the load on the Jog dial

It is the mode which judges the load (light/-- heavy) numerically when rotating JOG dial.
If it goes into the above-mentioned check mode of button and display function of the display part, a TOUCH/RELEASE knob is made in the maximum (right-hand side) and arbitrary buttons are pushed once, it will become JOG load check mode and top speed and time will displayed on a dot-matrix part.





Measuring method

In this state, if you rotate the Jog dial rapidly either clockwise or counterclockwise, figures are displayed.
For example, if "16.14 0135" is displayed, it means as follows:
16.14: Highest speed (given that the normal [1x] speed is when it takes 1.8 sec for the Jog dial to rotate one full turn.)
0135: Time (msec) required for the Jog dial to decrease its speed from 3x speed to 1.5x speed

As to the time required for the Jog dial to decrease its speed, if the measurement is performed for several times repeatedly, from the second measurement and afterward, the average of the current required time and the previous required time is displayed. Thus, after several measurements, the result becomes closer to the mean.

Notes

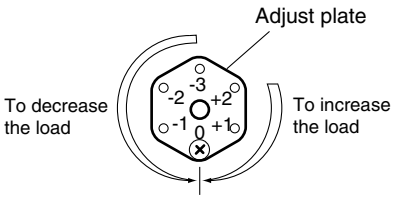
- Perform the measurement of load on the Jog dial more than three times.
- The measurement result is displayed only when the Jog dial is rotated 7 times normal speed "07.00" or more.

Management value

Jog management value: 150 ± 25 (msec)

Load adjustment method

Remove the screw fixing the adjust plate, then screw it into the hole corresponding to the value (-1, -2, -3, +1, or +2) for a load to be added:
-1, -2, -3 : To decrease the load
+1, +2 : To increase the load



JOG Check Mode : CANCEL

7. GENERAL INFORMATION

7.1 DIAGNOSIS

7.1.1 SERVICE MODE

1.The outline in service mode

This machine is controlled by two microcomputers, a display microcomputer and a player microcomputer, and test mode is prepared for each. A display microcomputer performs processing to a button input, display of FL, and lighting of LED. A player microcomputer drives a player.

[1] Check mode of a button and a display function of a display microcomputer.
It is the mode which checks a button input and a display function.

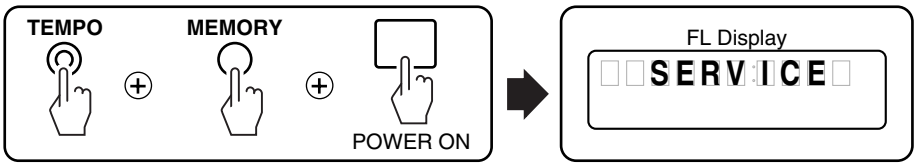
[2] Check mode of the load of JOG dial
It is the mode which measures the load when rotating JOG dial.

[3] Check mode of operation of a player microcomputer
It is the mode which performs the check of the mechanism and serbo of a player microcomputer of operation.
This mode consists of "player operation mode" and "test operation mode."

[4] Version check mode
It is the mode which can check the version of the software of each microcomputer.

[5] Error display list / Error display mode
The history of the contents of an error can be checked to 16 pieces.

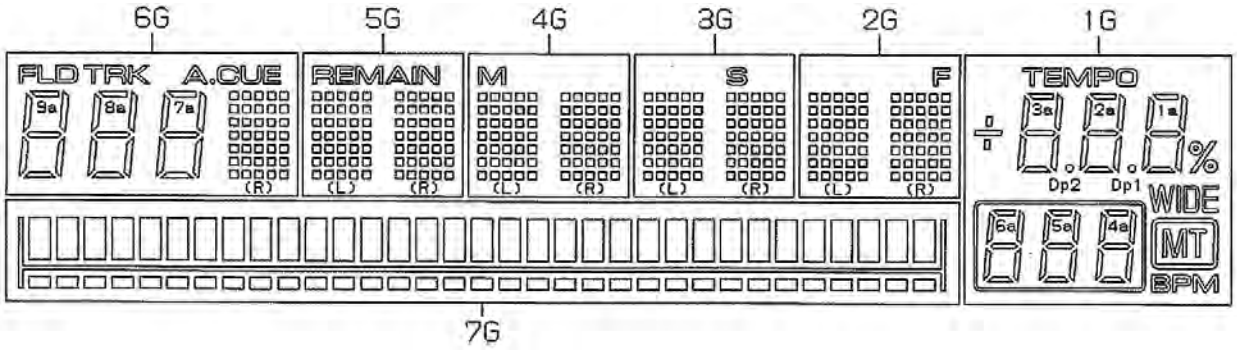
2.Check mode of a button and a display function of a display microcomputer.

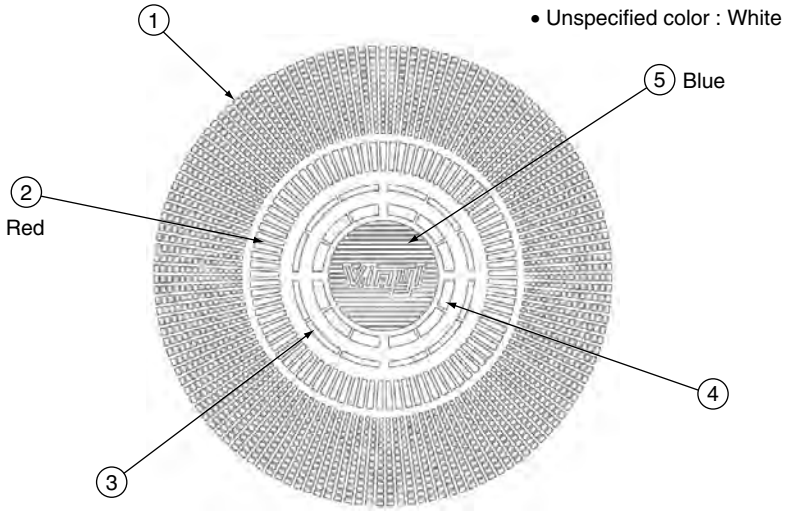


In this mode, it can check whether a display microcomputer can be made to turn on partially as follows, the input of each button and volume is normal, and a display is normal. In addition, a display is turned on only while pushing the button.

If a TOUCH/RELEASE knob is made into states other than the maximum (right-hand side), it will become the check mode of button and display function, and if each button is pushed, FL display and LED which correspond light up.
Moreover, if a knob is made into the maximum (right-hand side) and arbitrary buttons are pushed once, it will become JOG load check mode and top speed and time will be displayed on a FL dot-matrix part. (After-mentioned)

Button, Switch	FL Dot-matrix display	FL Other display	Light up LED
PLAY/PAUSE	PLAY		PLAY/PAUSE
CUE	CUE		CUE
IN/REALTIME CUE	IN		IN/REALTIME CUE
OUT/OUT ADJAST	OUT		OUT/OUT ADJAST
RELOOP/EXIT	RELOOP		RELOOP
FOLDER <-	FOLDER <-		
FOLDER ->	FOLDER ->	1G lights up	
TRACK (I<<)	TRACK I<<		
TRACK (>>I)	TRACK >>I	(1)	
REV (<<)	REV <<	(2)	
FWD (>>)	FWD >>	(3)	
BEAT LOOP 1	BEAT 1		BEAT LOOP 1
BEAT LOOP 2	BEAT 2		BEAT LOOP 2
BEAT LOOP 4	BEAT 4		BEAT LOOP 4
BEAT LOOP 8	BEAT 8		BEAT LOOP 8
JOG MODE	JOG MODE		VINYL
TEMPO	TEMPO	(5)	TEMPO 10%/WIDE
MASTER TEMPO	MASTER TE		MASTER TEMPO
QUICK RETURN	QUICK RET		QUICK RETURN
TIME MODE/AUTO CUE	TIME/ACUE		
TEXT MODE	TEXT MODE		
DELETE	All FL lights up	All FL lights up	All LED lights up
MEMORY	MEMORY		
EJECT	EJECT		
CUE/LOOP CALL <	CALL <		
CUE/LOOP CALL >	CALL >		
REVERSE	REVERSE		
TOUCH SENSOR	TOUCH SW	(4)	REV
JOG rotating to FWD	JOG >		
JOG rotating to REV	< JOG		



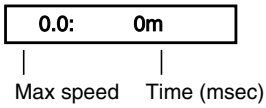


A display of TOUCH/RELEASE and TEMPO slider reading value

TOUCH/RELEASE and the TEMPO slider reading value is displayed in the form of a bar in 7G area of FL display part.
CUE Area : If a TOUCH/RELEASE knob is turned to the right, the number of display dots will increase.
Playing Address : If TEMPO slider knob is moved to + side, the number of display dots will increase.

3.Check mode of the load of JOG dial

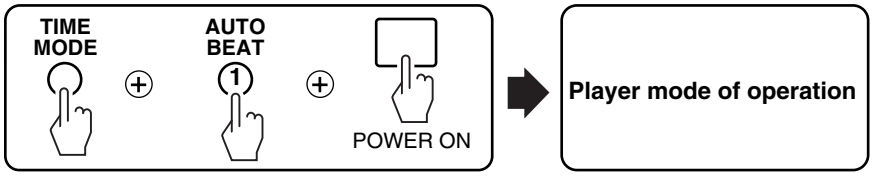
It is the mode which judges the load (light/-- heavy) numerically when rotating JOG dial.
If it goes into the above-mentioned check mode of button and display function of the display part, a TOUCH/RELEASE knob is made in the maximum (right-hand side) and arbitrary buttons are pushed once, it will become JOG load check mode and top speed and time will displayed on a dot-matrix part.



It goes into this mode, and a number will be displayed if JOG dial is turned with sufficient vigor.
the rotation direction -- right-handed rotation and left-handed rotation -- either is O.K.
For example, when displayed as "8.6: 115", the following contents are shown, respectively.
8.6 = What time speed came out by the highest. (The time of turning one rotation in 1.8 seconds is made into 1 time.)
115 = Time taken for rotation to fall by 1.5 times from 3 times (msec)

It is necessary to make it rotate top speed to 7.0 or more times to measure the rotation fall time required.
When it carries out continuously several times, the time which took the average with a part for greatest ever 4 time is displayed 2nd henceforth. Measurement which absorbed variation can be performed by performing this.

4.Check mode of operation with a player microcomputer simple substance



This mode consists of "player operation mode" and "test operation mode."

〈 **Player oparation mode** 〉
Basic operation of SABO, such as setup, play, pause, and track search, is carried out.
Moreover, measurement of an error rate can also be performed.

〈 **Test opalation mode** 〉
Serbo operation is finely controllable gradually.
* It becomes player operation mode and shifts to test operation mode by the key input in the beginning.
* The command treated here is for mainly testing a mechanism and a servo system, and is not for DJ functions, such as scan and tempo.

Function	The button of the main body
〈 **Player oparation mode** 〉	
Play(trace) / Pause	PLAY/PAUSE
Track Search F/R	TRACK SEARCH F/R
Error Rate Count	CUE
Eject	EJECT
Mode Change	MASTER TEMPO
〈 **Test opalation mode** 〉	
Servo All Off	TIME
LD On/Off	TEMPO
Focus On/Off	RELOOP
Spindle Kick, Tracking On/Off	LOOPIN
Tracking Off	LOOPOUT
Slide FWD (2mm)	SEARCH FWD
Slide REV (2mm)	SEARCH REV
Pickup Up/Down	TEXT
Mode Change	MASTER TEMPO

♦ **Player operation mode command**

Play(trace) / Pause
If it is in a stop state, it will set up and play.
Moreover, if it is in a play state, whenever it will push a button, a pause and a play are carried out by turns.
The address under present reproduction is displayed on FL.
* In this mode, even if it inserts a disk, an automatic setup is not carried out.
Moreover, a play is not carrying out audio reproduction, but is tracing the signal side of a disk.
At a play, a disk is traced by 4X rotation. A sound is not outputted.

Track Search F/R
It searchs in the direction of FWD or REV and stops in of the displayed track.

Error Rate Count
The error rate for about 10 seconds after the present position currently played is measured, and it displays on FL.
Usually, a track to measure is made to search and this button is inputted from a pause state.
For example, it is displayed as "3.56E-4 O.K." etc.
If an error rate is less than 3.00E-3, it will be displayed as O.K. If an error rate is larger than 3.00E-3, it will be displayed as NG.
Measurement with the managed disk at the time of factory shipments is a premise.
The product does not judge whether they are inferior goods at the time of service.

Eject
A disk is ejected.

Mode Change
If the MASTER TEMPO button is pushed into player operation mode, MASTER TEMPO LED will light up, and it will shift to the below-mentioned "test operation mode."

♦ **Test operation mode command**

Serbo operation is sinely controllable gradually.
Keep in mind a test operation mode command that it may give a gamage to a player sa mistaking the usage.

Servo All Off

When serbo is ON, all serbo will be turned off if the TIME button is pushed.

LD On/Off

If the TEMPO button is pushed, On and Off of LD will change.

Focus On

If the RELOOP button is pushed when having stopped, LD will be turned on and an auto focus will be performed.

Spindle Kick, Tracking On/Off

If the LOOP IN button is pushed into tracking serbo OFF, a spindle kick is performed and automatic adjustment processing and tracking serbo are turned on. Moreover, tracking serbo is turned off if it pushes into tracking serbo ON.

Tracking Off

Tracking serbo is turned off if the LOOP OUT button is pushed into tracking serbo ON.

Slide FWD

If the SEARCH FWD button is pushed into tracking serbo ON, tracking serbo will be turned off and a slider will be moved in the FWD direction about 2mm.

Slide REV

If the SEARCH REV button is pushed into tracking serbo ON, tracking serbo will be turned off and a slider will be moved in the REV direction about 2mm.

Pickup UP/DOWN

If an TEXT button is pushed when stopped, LD will be turned on and a pickup will be moved up and down.
A focus is not made to close.

Mode Change

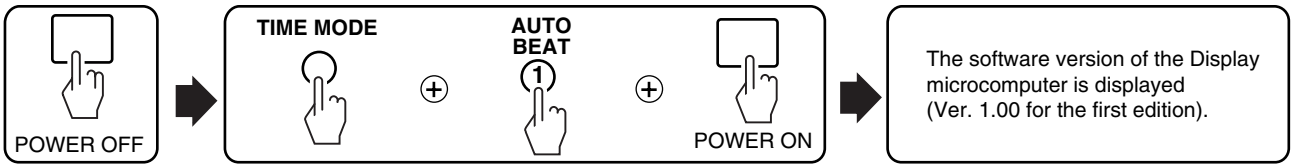
If the MASTER TEMPO button is pushed into "player operation mode", MASTER TEMPO LED will light up, and it will shift to the below-mentioned "test operation mode."

* When you rise at a step in test mode, please input a command in order of "Servo All Off", "Focus On", and "Spindle Kick, Tracking On."

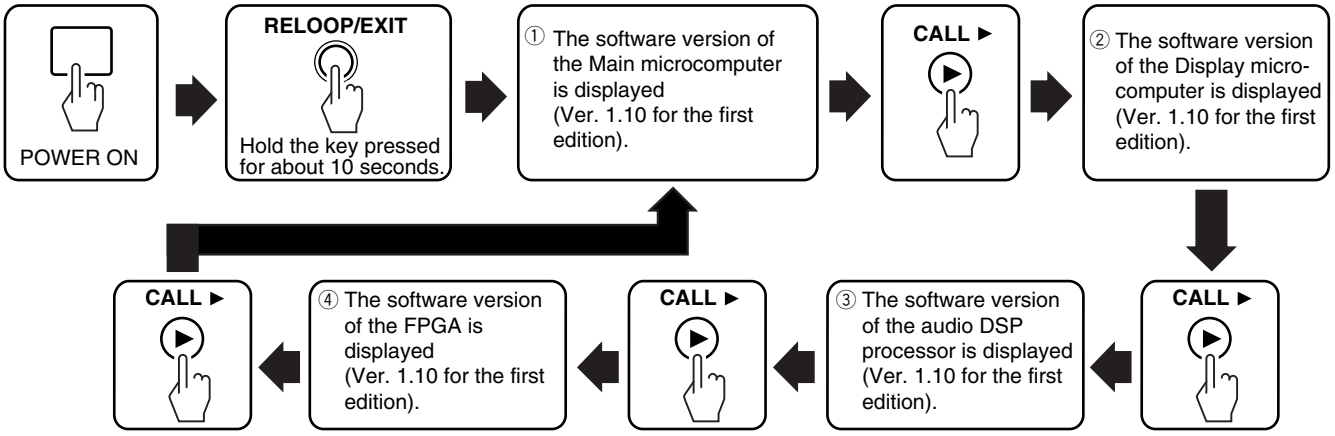
5. Version Check mode

Mode for checking the software version of each microcomputer

• How to check the software version of the Main microcomputer


POWER OFF
TIME MODE
AUTO BEAT
1
POWER ON
The software version of the Display microcomputer is displayed (Ver. 1.00 for the first edition).

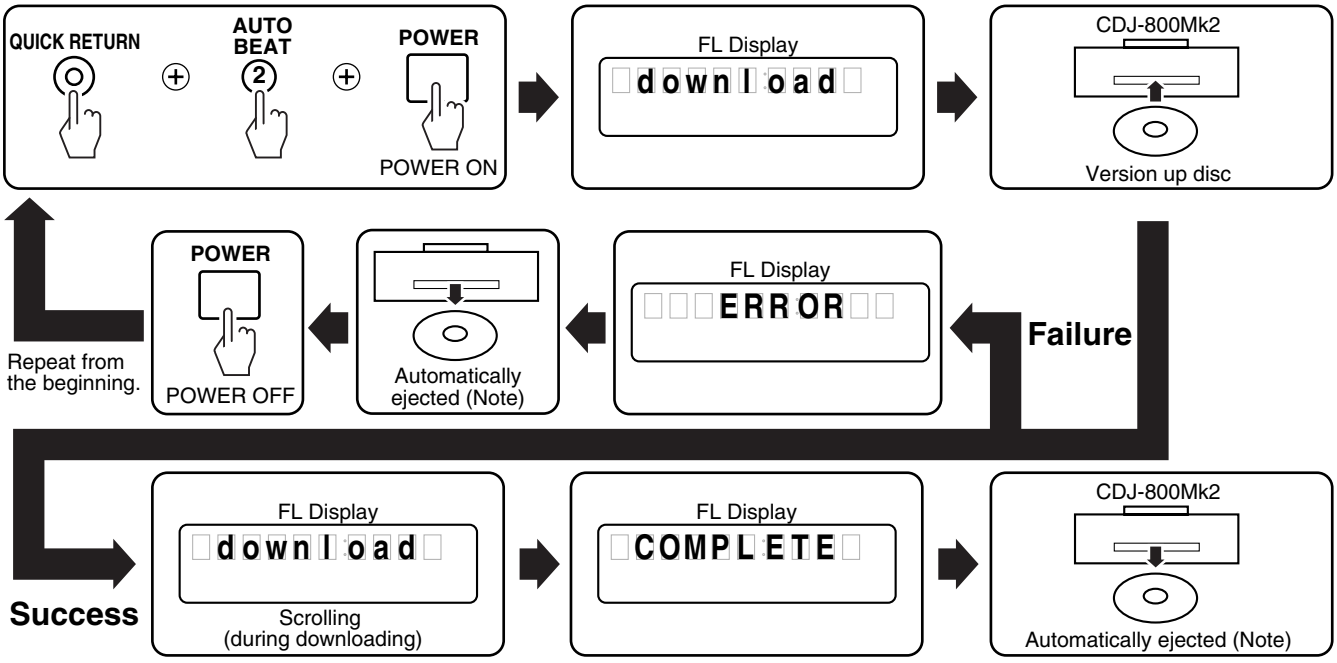
• How to check the software version of the Player microcomputer


POWER ON
RELOOP/EXIT
Hold the key pressed for about 10 seconds.
① The software version of the Main microcomputer is displayed (Ver. 1.10 for the first edition).
CALL ►
② The software version of the Display micro-computer is displayed (Ver. 1.10 for the first edition).
CALL ►
③ The software version of the audio DSP processor is displayed (Ver. 1.10 for the first edition).
CALL ►
④ The software version of the FPGA is displayed (Ver. 1.10 for the first edition).
CALL ►

[1] Ver. 1.00 The version of the microcomputer of a player part (main microcomputer).
[2] disp 1.00 The version of the microcomputer of a display part.
[3] DSP 1.00 The version of the audio DSP.
[4] FPGA 1.00 The version of the FPGA.

∗ Audio DSP and FPGA are the processors which performs audio processing and various signal control, and operates independently with a player microcomputer. However, the program is stored in FLASH-ROM of a player microcomputer, and has structure transmitted to each processor from a player microcomputer at the time of a power supply ON.

• How to upgrade the software of the microcomputer



Note:

- Do NOT turn off the power after the upgrade disc is loaded till it is automatically ejected. If you do, the unit may not operate properly afterward.
- Eject a disc automatically even if updating fails.

6. Error display list / Error display mode

When it cannot operate normally in the usual use, the following error numbers are displayed on a display part.
Moreover, at the time of the mode of the above-mentioned "check of the software version of a player microcomputer", if a JOG MODE button.
is pushed, a detailed error (E-XX which is the number of the "contents of an error" of the following table) can be checked.
Whenever it pushes JOG MODE button, "a version display" and "an error display" are changed by the toggle.
The error which pushed JOG MODE button and appeared first is the newest error. And the past error is displayed by pushing the CALL REV button (a push on the CALL FWD button displays the oldest error).
The error is memorized to 16 pieces.

Moreover, only "E-12" and "E-15" memorize the place (TNO : MIN:SEC:FRM) which the error generated. And it can change with the TIME button. (Toggle operation)

Error number	Error name	The contents of an error
E-6002	DSP PROGRAM DOWNLOAD ERROR	A program cannot be written in DSP.
E-7201	TOC READ ERROR	26: TOC data cannot be read.
E-8301	PLAYER ERROR (Starting is unusual.)	12 : A desired address has not been searched. 15 : An address cannot be read. 22 : Focal serbo cannot be closed. 91 : A pickup does not return to an inner circumference. } (∗Notes
E-8302	PLAYER ERROR (Reproduction is unusual.)	12 : A desired address has not been searched. 15 : An address cannot be read. 22 : Focal serbo cannot be closed.
E-8303	PLAYER ERROR (The writing of a buffer is unusual.)	99: The writing of a buffer is unusual.
E-8304	MP3 DECODE ERROR (The abnormalities of decoding)	Decoding is unusual.
E-8305	DATA FORMAT ERROR (The format of data is unusual.)	The format of those other than MP3
E-8709	COMMUNICATION ERROR	Communication of the microcomputer of a display part and the microcomputer of a player part cannot be performed.
E-9101	MECHANICAL TIME OUT	90: A disk loading mechanism's abnormalities (Timeout).

∗ Notes : (1) Before a disk is recognized to be CD, when these errors take place, a disk is ejected automatically. Although an error number is not displayed at this time, since the contents of an error are stored in the memory, please refer to it.
(2) E-8304 and E-8305 are not memorized by the internal memory.

An error history is clearable if a power supply is switched on pushing the QUICK RETURN button and the BEAT[4] button together.
At this time, a setup of AUTO CUE and TIME MODE turns into a setup at the time of factory shipments together.
(AUTO CUE LEVEL=-60dB, TIME MODE=REMAIN)

∗ CAUTIONT There is a function which carries out the memory of the CUE/LOOP point for the 800 maximum disks in this machine. If an error history is cleared, since all CUE/LOOP memories will also be cleared simultaneously, please take great care about use in this mode.

CDJ-800MK2 RESET ROOT MAP

MAIN ASSY

A **RESET I C**
BU4230G
IC304
DETECT VOLTAGE 3.0V
DELAY TIME 70ms

DC3.3V

XRST

1 **MPU**
SCF5249VM140
AMADEUS
IC301

PRGM

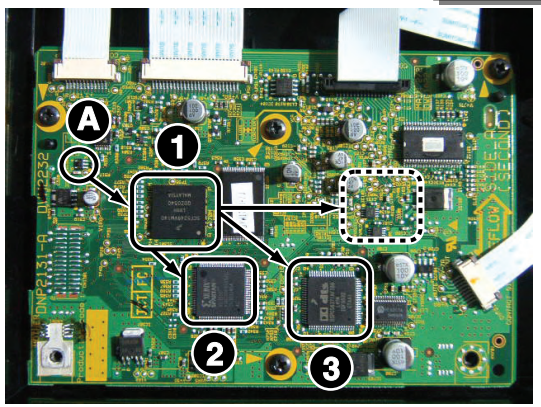
2 **FPGA**
XC3S50-4VQG100C
SPARTAN3
IC302

DSPRST

3 **DSP**
DSPC56371AF180
IC701

SRVRST

4 **ServoDSP**
TC94A15FG
IC101



A MAIN ASSY

B .DFLB
RESET I C
BU4242G
IC502
DETECT VOLTAGE 4.2V
DELAY TIME 70ms

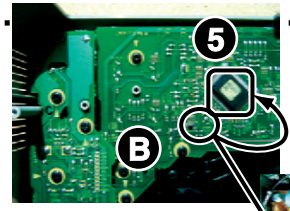
DC5V

XRST

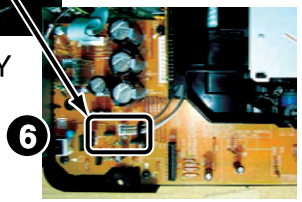
5 .DFLB
DISPLAY MPU
M16C/30P Series
PEG237B
IC501

XRST

6 .SECB
PowerSupply CIRCUIT VLD



G DFLB ASSY



C SECB ASSY

※ The RESET-LINE name is same as NET-NAME of schematic.

CDJ-800MK2 CLOCk DELIVERY MAP

MAIN ASSY

Ⓐ.TC7WU04FU

CPU16M

MPU
SCF5249VM140
AMADEUS
IC301

70MHz

70MHz

SDRAM
K4S641632K-UC75
HY57V641620ETP-H

CLK

VSS1084-A
16.9344MHz

X'TAL
FUNDAMENTAL
Tolerance±50ppm
Temp. Drift±50ppm

Output current adjustment is possible instead of the buffer by way of the FPGA inside, and suppress the return-loss by outputting a clock from different port.

70MHz and 16MHz do not interfere in the FPGA inside. (Other block)

FP16M

Output a clock only in the display data transmission.

FPGA
XC3S50 Series
SPARTAN-3
IC302

DSP16M

16MHz

DSP
DSPC56371AF180
IC701

DAC11M

11MHz

DAC
PE8001A
IC702

DFLB

DATA-FL
DEL1059-x

FLSCLK

1.6MHz

DFLB

DISPLAY
MPU
M16C/30P Series
PEG237B
IC501

TSCLK

1MHz

JFLB

JOG-FL
DEL1058-x

JSCLK

400kHz

SRV16M

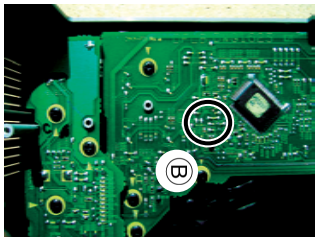
16MHz

ServoDSP
TC94A15FG
IC101

Ⓑ.DSS1149-A
16.000MHz

X'TAL
FUNDAMENTAL
Tolerance±20ppm
Temp. Drift±30ppm

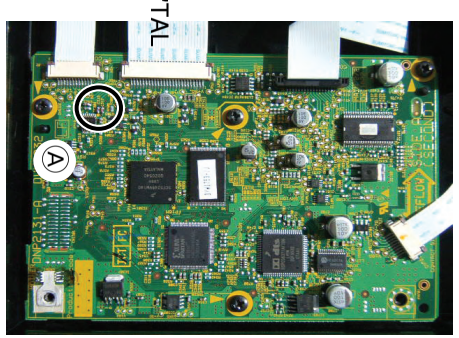
G DFLB ASSY



X'TAL

A MAIN ASSY

X'TAL



※ ····· : Discontinuous Clock Line
※ ◆ : The current of line is possible to drive variable.
※ The CLOCK-LINE name is same as NET-NAME of schematic.

7.1.3 TROBLE SHOOTING

Note : The numbers for the waveform photos are identical to those for the schematic diagrams and board diagrams.

Points to be checked beforehand and a note :

- When a failure judgment of the ICP (Micro Fuse) is performed using a tester, be sure to judge according to the resistance values. If a simplified measurement method, such as Short-circuit Check mode, is used for testing, a partially-damaged ICP cannot be detected.
- The ICP is very sensitive. First, check the power line to verify that the placed ICP is not damaged.
- Defective soldering of surface mount devices may have caused a problem. Check if the symptom changes when you press the corresponding surface mount device with a finger.
- For the address-bus and data-bus lines on the MAIN Assy, the dump (serial) resistance is never used.

Freeze (1/2)

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
E8709 error If the power supply is normal, this symptom is caused either by a defective core block of the MAIN Assy or a failure in communication between the DISPLAY MPU (IC501) and MAIN Assy. A defective core block means that the processes up to the FPGA (IC302) configuration have not been completed. In a case of a failure in the communication line, the core block is normal. In either case, no error indication is displayed on the control panel because the E8709 error code is sent to the DATA-FL display by the DISPLAY MPU itself. **Note:** The core block comprises 4 main ICs: MPU (IC301), SDRAM (IC303), FLASH (IC300), and FPGA (IC302).				 Control panel
		❶ Play back a CD. Check if the audio signal is output from the analog output terminal (JA801).	If the audio signal is output, the core block is OK. The cause is a failure in communication between the DISPLAY MPU and the MAIN Assy. On the contrary, if the CD cannot be played, the core block is in failure. Proceed to Step ❺.	
DFLB Assy SECB Assy		❷ Disconnect then reconnect the FFC cable between the DFLB and SECB Assys, and that between the SECB and MAIN Assys to check if the symptom is ameliorated.	If the symptom is ameliorated, loose connection of the FFC cable is the cause.	
Unit		❸ Disconnect then reconnect the FFC cable between the MAIN and JACK Assys and the cable with connectors that connects the JACK and SECB Assys to check if the symptom is ameliorated. Also check for the 5 V power line, including loose connection of the connectors.	If 5 V power is not supplied to the DAC (IC702), the 3-wire serial signal level between the DAC and the MPU is lowered, because the DAC is not started, which will lead to a failure in starting of the FPGA (the loading motor rattles). Repair the 5 V power line.	
DFLB Assy SECB Assy MAIN Assy	DFLB Assy ④ to ⑦	❹ Check the waveform at the points (TSCLK, TSDO, TSDI, and TSCS) designated in the waveform photo to confirm that the communication line between the DISPLAY MPU (IC301) and FPGA (IC302) is normal.	If the waveform is unstable or extremely low in level, loose connection of the output terminals or connectors on the line, chip fracture, poor power supply to IC308, or partial damage of IC308 may be the cause. Replace IC308 and check the connections.	
		❺ 5 Deployment of the data that had been written in the flash memory (IC300) into the SRAM built into the MPU (IC301) may have failed. Check that the voltage at TP19 is 0 V.	If the waveform at TP19 continuously fluctuates, deployment of the data failed. A checksum error of the SRAM built into the MPU (IC301) was generated. Check the mounting status of IC301.	
		❻ 6 Deployment of the program and data that had been written in the flash memory (IC300) into the SDRAM (IC303) may have failed. Check that the voltage at TP30 is 0 V.	If the waveform at TP30 continuously fluctuates, deployment of the program and data failed. A checksum error of the SDRAM (IC303) was generated. Check the mounting status of IC303.	
MAIN Assy		❼ Check if the soldered portion of IC311 on the CLK line is lifted off the board. Note: It has been found that the cell and the part are not compatible. With the Assys of the lots before the modification, defective mounting may have occurred.	If the defective mounting of IC311 is the cause, "POWER ON" is displayed for a while, a rattle is generated from the player, then E8709 error is indicated. A disc cannot be loaded in the player.	
MAIN Assy		❽ Check if the soldered portion of IC312 on the PRGM line is lifted off the board. Note: It has been found that the cell and the part are not compatible. With the Assys of the lots before the modification, defective mounting may have occurred.	If the defective mounting of IC312 is the cause, "POWER ON" is displayed for a while, then E8709 error is indicated. A disc cannot be loaded in the player.	
MAIN Assy SECB Assy REGB Assy		❾ Check the power system for the core block, paying attention to the following points: (1) Is the ICP damaged?, and (2) Are cables firmly connected?	Replace the ICP or check the cable connections.	
TRNS Assy ACIN Assy		❿ If power is not supplied to any power system, check the primary source. Inappropriate commercial power input or blown primary fuse (FU8001) or transformer fuse (T21) may be the cause.	Replace the fuses.	
MAIN Assy	MAIN Assy ⑱	⓫ Check the waveform at the RST Test Land, referring to the waveform photo, to confirm that the Reset IC (IC304) resets the MPU (IC301) properly. The Reset IC is normal if resetting is canceled about 70 msec after the power is turned on.	Abnormal delay time or an unstable waveform suggests fracture of the C303 chip. Replace the C303. If the symptom is not ameliorated, replace the IC304.	

Freeze (2/2)

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
MAIN Assy	MAIN Assy ⑦①	⓬ Check the waveform at the CPU16M Test Land, referring to the waveform photo, to confirm that the crystal oscillation circuit is operating normally.	An unstable waveform or extremely low level suggests chip fracture or partial damage of the crystal oscillator (X301). Replace the chip or X301.	
MAIN Assy	MAIN Assy ⑲	⓭ Check the waveform at the designated point on the PRGM line, to confirm that the MPU (IC301) resets the FPGA (IC302) properly.	An unstable waveform suggests loose connection of the output terminal of the MPU (IC301) or chip fracture on the PRGM line. Even if the waveform at the designated point is	
MAIN Assy	MAIN Assy ㉓ to ㉚	⓮ Check the waveform at the point designated on the waveform photo, to confirm that the configuration procedures between the MPU (IC301) and FPGA (IC302) are properly performed.	An unstable waveform suggests loose connection of the output terminal or chip fracture. Even if the waveform at the designated point is normal, there may be poor contact of connectors in downstream lines. Resolder the output connectors,	

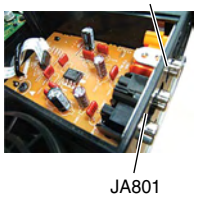
Display (1/2)

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
Lighting of the LEDs and indications and the FL display on the control panel do not function. If the power supply is normal, this symptom is caused by a defective DISPLAY MPU (IC501,) which controls the display on the control panel, including the FL indication and lighting of the LEDs. (If the DISPLAY MPU is normal, the indications of internal data on the DISPLAY MPU, such as POWERON and E-8709, will be displayed on the DATA-FL display.) To confirm that the core block of the MAIN Assy is normal, play back a CD without using the control panel and check the audio output.				
DFLB Assy SECB Assy REGB Assy		❶ Check the power to be supplied to the control panel, paying attention to the following points: (1) Is the ICP damaged?, and (2) Are cables firmly connected?	Replace the ICP or check the cable connections.	
TRNS Assy ACIN Assy		❷ If power is not supplied to any power system, check the primary source. Inappropriate commercial power input or blown primary fuse (FU8001) or glass fuse (T21) are possible.	Replace the fuses.	
DFLB Assy	DFLB Assy ㊾	❸ Check the waveform of the XRST line, referring to the waveform photo, to confirm that the Reset IC (IC502) resets the DISPLAY MPU (IC501) properly. The Reset IC is normal if resetting is canceled about 70 msec after the power is turned on.	Abnormal delay time or an unstable waveform suggests fracture of the C507 chip. Replace the C507. If the symptom is not ameliorated, replace the IC502.	
DFLB Assy	DFLB Assy ⑦②	❹ Check the waveform at Pin 12 of IC501, referring to the waveform photo, to confirm that the crystal oscillation circuit is operating normally.	An unstable waveform or extremely low level suggests chip fracture or partial damage of the crystal oscillator (X501). Replace the chip or X501.	
No indication only on the DATA-FL display If the power supply is normal, this symptom can be caused only by a failure in the DATA-FL (V501) or the communication between the DATA-FL and DISPLAY MPU (IC501).				
		❶ Enter Display Check mode of Service mode and check if other keys on the control panel function and if the LEDs light.	If the LEDs and JOG-FL (V601) do not light, nor does the DATA-FL (V501) display, the DISPLAY MPU that controls those will not function properly. See "Lighting	
ACIN Assy		❷ Check the setting of the voltage selector switch (on the rear panel). (for RLF model)	Set the switch to the position that corresponds to the commercial power source.	
DFLB Assy SECB Assy TRNS Assy		❸ Check the Vload voltage (VLD, VLDD). If the voltage measured at the periphery of the power terminal of the DATA-FL (V501) is 29.3 V DC or more, it is OK.	If the voltage is 0 V, the ICPs (IC25, IC58, and IC59) are fried. Replace the ICPs.	
DFLB Assy	DFLB Assy ⑦④	❹ Check the FLAC voltage (FLAC1, FLAC2). If the voltage measured at the both ends of the DATA-FL (V501) lead is 4 V AC or more, it is OK.	If the AC current waveform does not appear, check the connection between the Assys.	
DFLB Assy		❺ Check the waveform at Pin 46 of DATA-FL (V501), to confirm that 5 V power is supplied to the built-in driver.	If the 5 V power is not supplied, soldering touchup is needed.	
DFLB Assy	DFLB Assy ⑤④ to ⑤⑦	❻ Check the points designated in the waveform photo to confirm that the procedures of the communication between the DISPLAY MPU (IC501) and the DATA-FL (V501) are normal.	A solder fracture of the DATA-FL terminal or loose connection of the terminals on the communication line between the DISPLAY MPU and the DATA-FL is suspected. Soldering touchup is needed. If the symptom is not ameliorated after soldering touchup, replace the DATA-FL.	

Display (2/2)

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
No indication only on the JOG-FL display If the power supply is normal, this symptom can be caused only by a failure in the JOG-FL (V601) or the communication between the JOG-FL and the DISPLAY MPU (IC501).				
		❶ Enter Display Check mode of Service mode and check if other keys on the control panel function and if the LEDs light.	If the LEDs and DATA-FL (V501) do not light, nor does the JOG-FL (V601) display, the DISPLAY MPU that controls those will not function properly. See "Lighting of the LEDs and indications and the FL display on the control panel do not function."	
ACIN Assy		❷ Check the setting of the voltage selector switch (on the rear panel). (for RLF model)	Set the switch to the position that corresponds to the commercial power source.	
JFLB Assy DFLB Assy SECB Assy TRNS Assy		❸ Check the Vload voltage (VLD, VLDD, VLDJ). If the voltage measured at the periphery of the power terminal of the JOG-FL (V601) is 27.8 V DC or more, it is OK.	If the voltage is 0 V, the ICPs (IC25, IC58, IC59, and IC603) are fried. Replace the ICPs.	
JFLB Assy		❹ Check the FLAC voltage (FLAC3, FLAC4). If the voltage measured at the both ends of the JOG-FL (V601) lead is 2.6 V AC or more, it is OK.	If the AC current waveform does not appear, check the connection between the Assys.	
JFLB Assy		❺ Check the waveform at Pin 23 of JOG-FL (V601), to confirm that 5 V power is supplied to the built-in driver.	If the 5 V power is not supplied, soldering touchup is needed.	
JFLB Assy	JFLB Assy ⑥⓪ to ⑥③	❻ Check the points designated in the waveform photo to confirm that the procedures of the communication between the DISPLAY MPU (IC501) and the JOG-FL (V601) are normal.	A solder fracture of the JOG-FL terminal or loose connection of the terminals on the communication line between the DISPLAY MPU and the JOG-FL is suspected. Soldering touchup is needed. If the symptom is not ameliorated after soldering touchup, replace the JOG-FL.	
No indication on either the DATA-FL nor JOG-FL displays This symptom occurs when the Vload voltage, to be supplied to both the DATA-FL (V501) and JOG-FL (V601), is not supplied.				
JFLB Assy DFLB Assy		❶ Check if the Vload voltage (VLD, VLDD, VLDJ) is supplied.	If the voltage is 0 V, the ICPs on the line are fried. Replace the ICPs.	
SECB Assy		❷ Check if the Vload power circuit is reset canceled. Check if the voltage at Pin 9 of CN56 becomes high after the power is turned on.	Resetting of this circuit is performed by the Reset circuit (IC502) mounted on the DLFB Assy. Resetting is done simultaneously with the DISPLAY MPU (IC501). As only the FL display has a problem, Pin 9 of CN501 on the DFLB Assy is in failure.	
Part of the FL display does not light, frequently flickers, or is dark.				
DFLB Assy JFLB Assy		❶ Visually check if the symptom occurs constantly in the same area.	If the symptom occurs constantly in the same area, the FL display is defective.	
JFLB Assy DFLB Assy SECB Assy TRNS Assy		❷ If the symptom does not occur in the same area, check the waveform of the Vload voltage, FLAC voltage and 5 V power, to confirm that the supply is stable. (See Steps ❸, ❺, and ❻ in "No indication only on the DATA (or JOG)-FL display.")	If the supply is unstable, soldering touchup is needed. If the symptom persists, replace the part.	
Black dots or stains appear on some parts of the FL display afer Display Check mode of Service mode is entered.				
			Impurities in the FL tube are the cause. For amelioration, replace the DATA-FL or JOG-FL.	

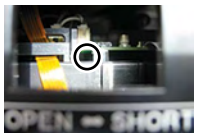
Audio output

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
No audio signal is output. If a signal waveform is normally output from the digital output terminal (JA802), the AUDIO DSP (IC701) is judged to be normal. In such a case, the problem exists at the subsequent stages of the AUDIO DSP output. During CD playback, first check the analog output terminal (JA801) then the previous stages. Be sure to carefully check for solder fractures at the phono plug.				
JACK Assy		❶ Check the waveform of the audio output signal at the analog output terminal (JA801). Check if the audio signal is not output from L and R channels, or only from one channel.		
JACK Assy		❷ Check if the digital audio signal is output from the digital output terminal (JA802).	If the digital audio signal is also not output, the AUDIO DSP (IC701) Assy is defective. See Step ❹ in "No digital output."	
JACK Assy	JACK Assy ㊵	❸ Check the waveform at the L4 and R4 Test Lands near analog output terminal (JA801).	If the audio signal is output from those points, a solder fracture of the phono plug or chip fracture on the audio line is suspected. Soldering touchup is needed.	
JACK Assy SECB Assy		❹ Check if 8 V and -7 V power are supplied to the OP AMP (IC801).	If the power is not supplied, check the cable connection of the power line.	
JACK Assy		❺ Check the waveform at the L1 and R1 Test Lands on the OP AMP (IC801).		
MAIN Assy	MAIN Assy ㊺	❻ Check the waveform at the Lch and Rch Test Lands near C705/C706.	If the audio signal is output at the point, audio muting may remain activated. During CD playback, check if the logical state of the signal at Pin 4 of CN801 is low.	
MAIN Assy		❼ Check if 5 V power is supplied to the DAC (IC702).	If the power is not supplied, check the cable connection of the power line.	
MAIN Assy	MAIN Assy ㉟	❽ Check the waveform at the 11M Test Land, referring to the waveform photo, to confirm that the clock input to the DAC (IC702) is normal.	An unstable waveform or extremely low level suggests loose connection of the clock terminal on the AUDIO DSP.	
MAIN Assy	MAIN Assy ㊶to㊸	❾ Check the points (DACLRCK, DACDATA, DACBCK) designated in the waveform photo to confirm if the procedures of the communication between the DAC (IC702) and AUDIO DSP (IC701) are normal.	An unstable waveform suggests loose connection output terminals on the AUDIO DSP or chip fracture on the line.	
Audio performance is poor. As grounding to the chassis is poor with this model, audio performance is largely affected if the specify screws are not tightened with the standard torque.				
		❶ Check if the screw that secures the bottom plate and is located near the plug is a screw with a projection (BBT).	Replace with a BBT screw if the original screw is not BBT.	
		❷ Check if the two screws that secure the bottom plate, including the above-mentioned screw with a projection, are firmly secured.	If the screws are loosely tightened, retighten the screws with the standard torque.	
Poor S/N ratio at the intervals of no sound, such as between musical pieces The S/N ratio is poor at the intervals of no sound, such as between musical pieces and at the time of power on, because audio muting is not activated. Possible causes are zero-data detection signals not output from the DAC (IC702) or a defective audio muting circuit. The following checks must be performed during CD playback.				
MAIN Assy	MAIN Assy ㊹	❶ Check the waveform at the terminal (Pin 21) for zero-data detection on the DAC (IC702). If the level is low between musical pieces and at the time of power on and high during CD playback, the terminal is normal.	If inversion of the logical state of signals is not performed, loose connection of Pin 21 on the DAC is most likely. Soldering touchup is needed.	
MAIN Assy	MAIN Assy ㊻	❷ Check the waveform at Pin 6 of CN701. If the level is high between musical pieces and at the time of power on and low during CD playback, the terminal is normal.	If audio muting remains deactivated, check chip fracture on the line or cable connection.	

Digital output

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
No digital output First, check if neither analog nor digital signals are output. If neither is output, the AUDIO DSP (IC701) is in failure. During CD playback, first check the digital output terminal (JA802) then the previous stages. Be sure to carefully check for solder fractures at the digital output terminal.				
JACK Assy		❶ Check the waveform of the digital audio signal at the digital output terminal (JA802).		
JACK Assy		❷ Check if the analog audio signal is output from the analog output terminal (JA801).	If neither digital nor analog audio signal is output, the AUDIO DSP (IC701) does not function properly. Proceed to Step ❹.	
MAIN Assy	MAIN Assy ⑦⓪	❸ Check the waveform at the point designated.	No signal suggests lifted soldered portion of the AUDIO DSP (Pin 69 of IC701) or chip fracture on the line. If there is a signal output, poor cable connection, loose connection of the connectors, or solder fracture of the phono plug is suspected.	
MAIN Assy	MAIN Assy ㉙	❹ Check the waveform at the DSP16M Test Land, to confirm that the 16 MHz clock signal is supplied from the MPU (IC301) via the FPGA (IC302).		
MAIN Assy	MAIN Assy ㉑, ㉖, ㉛, ㉜, ㉞, ㉟	❺ Check the waveform at the point designated, to confirm that the configuration procedures between the MPU (IC301) and the AUDIO DSP (IC701) are properly performed.	An unstable waveform suggests loose connection of the output terminal or chip fracture.	

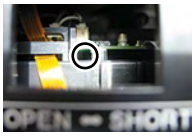
Player (1/4)

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
No disc playback. **A disc is ejected immediately after it is loaded. (without an error code)**				 LD short-circuit switch LD short-circuit land
RLYB Assy		❶ Visually check if the LD short-circuit switch (S1101) remains closed.	Set the LD short-circuit switch to OPEN.	
Player		❷ Check if the slot-in mechanism SV Assy is securely hooked to the player unit.	Firmly secure the Assy with the four hooks.	
Pickup Assy		❸ Visually check if solder is short-circuited at the LD short-circuit Land on the Pickup Assy.		
Unit		❹ Check if the FFC cables between the pickup and the RLYB Assy and the RLYB and MAIN Assys are improperly connected, if the conductor side is defective, and if there is poor contact, such as cable disconnection. Also check for loose connection of connectors.	If the symptom is ameliorated by replacement of the FFC cable, the defective cable is the cause.	
MAIN Assy		❺ Check the voltage of each section on the MAIN Assy.		
MAIN Assy		❻ Replace the MAIN Assy.		
A disc cannot be loaded.				
Unit		❶ Check if the FFC cables between the pickup and the RLYB Assy and the RLYB and MAIN Assys are improperly connected, if the conductor side is defective, and if there is poor contact, such as cable disconnection. Also check for loose connection of connectors.	If the symptom is ameliorated by replacement of the FFC cable, the defective cable is the cause.	
MAIN Assy		❷ Check the voltage of each section on the MAIN Assy.		
MAIN Assy		❸ Replace the MAIN Assy.		

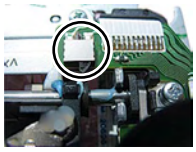
Player (2/4)

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
Loading-in attempts are repeated although no CD is loaded. (On the DATA-FL display, the indications "NO-DISC" and "EJECT" are alternately displayed.) **A CD cannot be loaded.** A failure in the detection system of the slot-in mechanism SV Assy is most likely the cause. The detection switch detects a trigger signal for operation start or stop of the loading motor. The present symptom may be caused by the disability of detection of a trigger signal for operation start.				
SLMB Assy		❶ Visually check if the loading detection switch (S1902) is kept pressed by the switch lever (white) as the lever overrides the switch.	Disengage the switch lever from the loading detection switch (S1902). If the detection switch is not closely seated on the board, soldering touchup is needed.	
MAIN Assy	MAIN Assy ③,④	❷ Check the SW signal at the LPS2 and LPS1 Test Lands at the time of CD loading, referring to the waveform photo. Does the SW signal change from L to H? Especially pay attention to a change at LPS2.	Repeated loading-in attempts may be caused by short-circuiting of the line to ground. Disabled CD loading may be caused by a solder fracture at the loading detection switch (S1902), soldered portion lifted off the board of the surface mount part on the line, or loose connection of the FFC cables.	
MAIN Assy	MAIN Assy ⑤	❸ By observing the waveform at the PWMLO Test Land, check that the duty at PWMLO changes, as indicated in the waveform photo: • During stop: Duty 50 % • During loading-in: Duty 0 % • During loading-out: Duty changes from 100 %, 25 %, then to 75 %.		
MAIN Assy		❹ Check the voltage at the MPU (IC301), FPGA (IC302), IC105 (TC7W04), and the driver IC (IC102).		
No ejection. Abnormal noise generated after a CD is loaded A failure in the detection system of the slot-in mechanism SV Assy is most likely the cause. The detection switch detects a trigger signal for operation start or stop of the loading motor. The present symptom may be caused by the disability of detection of a trigger signal for operation stop.				
MAIN Assy	MAIN Assy ③,④	❶ Check the SW signal at the LPS1 and LPS2 Test Lands at the time of CD loading, referring to the waveform photo. Does the SW signal change from L to H? Especially pay attention to a change at LPS2.	This symptom may be caused by short-circuiting of the line to ground. It may also be caused by a solder fracture at the loading detection switch (S1901), soldered portion lifted off the board of the surface mount part on the line, or loose connection of the FFC cables.	
MAIN Assy	MAIN Assy ⑤	❷ By observing the waveform at the PWMLO Test Land, check that the duty at PWMLO changes, as indicated in the waveform photo: • During stop: Duty 50 % • During loading-in: Duty 0 % • During loading-out: Duty changes from 100 %, 25 %, then to 75 %.		
MAIN Assy		❸ Check the voltage at the MPU (IC301), FPGA (IC302), IC105 (TC7W04), and the driver IC (IC102).		

Player (3/4)

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
The error rate measured in Test Operation mode of Service mode is high.				
		❶ To which the cause is attributed, disc or player, must be judged first. Visually check the disc for stains on the recording surface.	If the disc is clearly stained, replace it with a clean CD.	
		❷ Using the disc that produced a high error rate, measure an error rate at addresses in a different area.	If the error rate at addresses in a different area is not high, the CD is defective. Replace it with a high-quality CD. If the error rates at addresses in different areas on the whole disc are high, proceed to Step ③.	
Pickup Assy		❸ Check if shavings or dirt are attached to the pickup lens.	Clean the lens.	
Player		❹ Check if the TM Assy (servo mechanism) is securely attached.		
Player		❺ Check if the loading mechanism SV Assy is securely attached.		
Pickup Assy		❻ Check if any foreign object is on the spindle table.	Remove the foreign object.	
Pickup Assy		❼ Check if any foreign object is attached to the magnet section of the Pickup Assy.	Remove the foreign object.	
Player	MAIN Assy ①,②,⑧,⑪	❽ Check the S-curve, TE, RFO, and AGCRF levels in Service mode.	See "Failure judgment of the Pickup Assy" for details.	
The LD is not turned on after entering Test Operation mode of Service mode.				 LD short-circuit switch
RLYB Assy		❶ Visually check if the LD short-circuit switch (S1101) remains closed.	Set the LD short-circuit switch to OPEN.	
MAIN Assy		❷ Check that Pins 41 and 42 on the Servo DSP (IC101) are open or short-circuited.		
Player		❸ Check if the FFC cable that connects the Pickup and the RLYB Assys is securely connected to the Pickup Assy, if the conductor side is defective, and if there is any cable breakage. Also check for loose connection of connectors.	If the symptom is ameliorated by replacement of the FFC cable, the defective cable is the cause.	
MAIN Assy		❹ Check if the R101 to R105 or Q105 are missing.		
MAIN Assy		❺ Check if the FFC cable that connects the RLYB and MAIN Assys is firmly connected to CN101.		
The pickup lens does not move up or down after entering Test Operation mode of Service mode.				
Player		❶ Check if the FFC cable that connects the TM and the RLYB Assy is securely connected to the Pickup Assy, if the conductor side is defective, or if there is any cable breakage. Also check for loose connection of connectors.	If the symptom is ameliorated by replacement of the FFC cable, the defective cable is the cause.	
Pickup Assy		❷ Check if the resistance of the focus coil is too large or if the focus coil is broken, using Service mode.	See "Failure judgment of the Pickup Assy" for details.	
MAIN Assy		❸ Check if the 7 V power is supplied to Pin 32 of IC102.		
MAIN Assy	MAIN Assy ⑨	❹ Check if the signal output from the FOO terminal on the MAIN Assy oscillates centered around 1.65 V.		

Player (4/4)

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
The spindle motor does not rotate after entering Test Operation mode of Service mode.				
MAIN Assy		❶ Check if the FFC cable that connects the TM and MAIN Assys is securely connected to CN102, if the conductor side is defective, or if there is any cable breakage. Also check for loose connection of connectors.	If the symptom is ameliorated by replacement of the FFC cable, the defective cable is the cause.	
Player		❷ Check if the Loading Mechanism Assy operates normally. (Check if there is a clamping error or scratching noise of the disc.)		
MAIN Assy		❸ Check if 7 V power is supplied to R121 to R126 on the MAIN Assy.		
MAIN Assy	MAIN Assy ⑫	❹ Check if the PWM waveform that oscillates centered around 1.65 V can be observed for the DMO Test Land on the MAIN Assy.		
The slider does not move after entering Test Operation mode of Service mode.				 Inside switch
RLYB Assy		❶ Check if the FFC cable (stepper flexible cable) is connected to CN1104 on the RLYB Assy.		
MAIN Assy		❷ Because the slider does not move until the Inside signal is recognized, check if the FFC cable that connects the TM and MAIN Assys is securely connected to CN102, if the conductor side is defective, and if there is any cable breakage. Also check for loose connection of connectors.	If the symptom is ameliorated by replacement of the FFC cable, the defective cable is the cause.	
MAIN Assy		❸ Check if the signal at Pin 1 of CN102 becomes low when the power is turned on. (Is the Inside switch damaged?)		
MAIN Assy		❹ Check if power is supplied to IC102.		
MAIN Assy	MAIN Assy ⑮,⑯	❺ Check if a sine-wave signal is input to Pins 1 and 2 of IC102.		

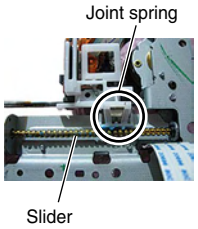
User setting

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
After the power is turned off, the user settings, such as AUTO CUE and TIME MODE settings, are cleared. With this model, the CUE point, AUTO CUE, and TIME MODE settings and error logs are stored in the flash memory on the MAIN Assy as user settings. No error indication is displayed for this symptom.				
MAIN Assy		After resetting the user settings to default in Service mode, set a CUE point while a CD is being played back. After the CUE point setting, wait at least 5 seconds and turn the power off then back on. Check if the CUE point is called.	Loose connection of the FLASH IC (IC300) connector is likely. If the symptom is not ameliorated after touching up the solder with a soldering iron, replace the FLASH IC.	

Updating

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
"ERROR" is displayed on the DATA-FL display. Updating of the firmware is possible in Service mode. All errors generated during updating are indicated as "ERROR," and updating fails.				
Player		❶ Check if a wrong CD has been loaded.	Use the correct CD for updating.	
Player		❷ Check if the recording surface of the disc is stained.	Replace with a clean CD for updating.	
RLYB Assy		❸ Visually check if the LD short-circuit switch (S1101) remains closed.	Set the LD short-circuit switch to OPEN.	
Pickup Assy		❹ Check if shavings or dirt are attached to the pickup lens.	Clean the lens.	
MAIN Assy		❺ After resetting the user settings to default in Service mode, set a CUE point while a CD is being played back. After the CUE point setting, wait at least 5 seconds and turn the power off then back on. Check if the CUE point is called.	Loose connection of the FLASH IC (IC300) connector is likely. If the symptom is not ameliorated after touching up the solder with a soldering iron, replace the FLASH IC.	

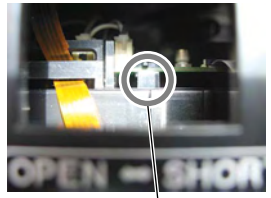
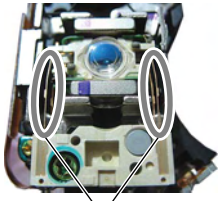
Error codes (1/2)

Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
E-6002 **DSP PROGRAM DOWNLOAD ERROR** At the time of initialization, the program was not downloaded (written) to the EEPROM on the AUDIO DSP. There may be a factor that hampers normal initialization of the EEPROM on the AUDIO DSP at the time of power on. The possible cause is defective state of 3-wire serial lines that are commonly used by the MPU and the FPGA, AUDIO DSP, and DACs. The data on this symptom are not stored in the internal memory.				
MAIN Assy	MAIN Assy ㉖,㉜, ㉞	Check the waveforms of the 3-wire serial lines (CLK, DATA, DSPDREQ) to confirm that the configuration procedures are properly performed.	Chip fracture or soldered portion of IC lead lifted off the board on the line where the waveform does not change is most likely the cause. In the former case, replace the chip. In the latter case, soldering touchup is needed.	
E-7201 **TOC READ ERROR** Table of Contents (TOC) data cannot be read. This symptom is associated with the reading accuracy of the servo motor of the CD player.				
Player		Measure the error rate in Player Operation mode of Service mode. To which the cause is attributed, disc or player, must be judged first. For measuring, play back the lead-in point indicated in the error code by listening the sound.	Follow the procedures described in "The error rate measured in Test Operation mode of Service mode is high."	
E-8301 **PLAYER ERROR (Startup error)** • E830112: The desired address could not be searched for. • E830115: The address could not be read. • E830122: The focus servo could not be closed. • E830191: The pickup did not return toward the inner tracks. If the above-mentioned error codes are indicated before the loaded disc is recognized as a CD, the disc will be automatically ejected. This symptom is associated with the reading accuracy of the servo motor of the CD player.				
Player		❶ Measure the error rate in Player Operation mode of Service mode. For the error codes other than E830191, proceed to Step ❸.		
MAIN Assy	MAIN Assy ⑩	❷ Check the waveform at the INSIDE Test Land near CN102, by changing the positions of the Inside switch. Does the signal change between low and high according to the switch settings?	If the signal does not change, a defective Inside switch, solder fracture, soldered portion lifted off of the surface mount on the line, and loose connection of the FFC cables are likely causes.	
Player		❸ Visually check if the joint spring on the TM Assy is deformed. Also check for the sliding smoothness of the slider.	If the joint spring is deformed or displaced or if the slider moves abnormally smoothly, replace the pickup.	
Player		❹ Measure the error rate in Player Operation mode of Service mode. To which the cause is attributed, disc or player, must be judged first. For measuring, play back the lead-in point indicated in the error code by listening the sound.	Follow the procedures described in "The error rate measured in Test Operation mode of Service mode is high."	
E-8302 **PLAYER ERROR (Abnormality in playback)** • E-830212: The desired address could not be searched for. • E-830215: The address could not be read. • E-830222: The focus servo could not be closed. This symptom is associated with the reading accuracy of the servo motor of the CD player.				
Player		Measure the error rate in Player Operation mode of Service mode. To which the cause is attributed, disc or player, must be judged first. For measuring, play back the lead-in point indicated in the error code by listening the sound.	Follow the procedures described in "The error rate measured in Test Operation mode of Service mode is high."	

Error codes (2/2)

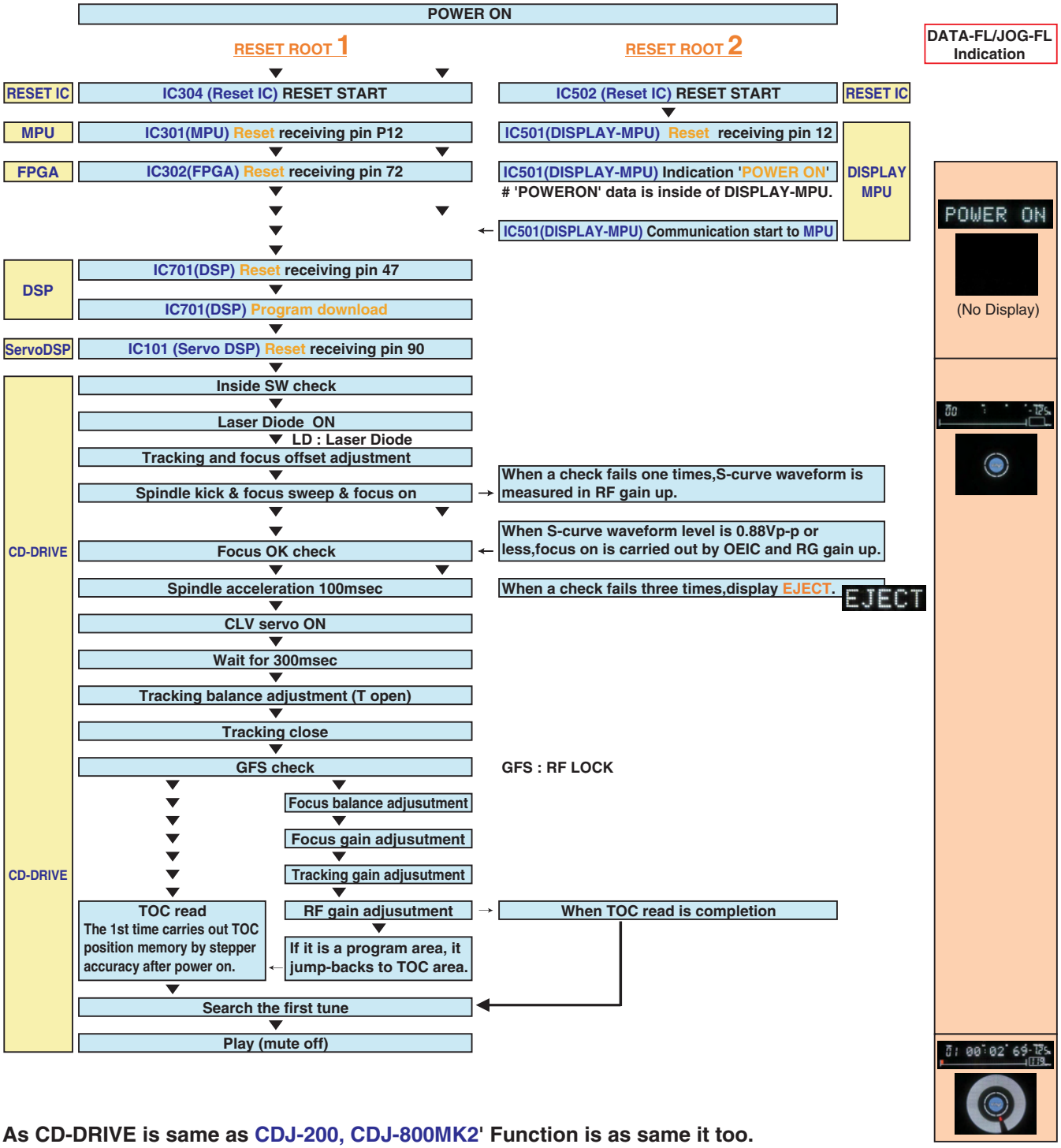
Sites	Waveforms	Points to be checked	Causes & Measures to be taken	Remarks
E-8303 **PLAYER ERROR (Abnormality in writing in the buffer)** • E830399: Abnormality in writing in the buffer In theory, this error code means that buffering to the SDRAM (IC303) was impossible. However, a defective SDRAM may not be a real cause, because the unit would freeze if the SDRAM were defective. This error code is generated by factors associated with the reading accuracy of the servo motor of the CD player, such as a high error rate and subcode not read.				
Player		Measure the error rate in Player Operation mode of Service mode. To which the cause is attributed, disc or player, must be judged first. For measuring, play back the lead-in point indicated in the error code by listening the sound.	Follow the procedures described in "The error rate measured in Test Operation mode of Service mode is high."	
E-8304 **MP3 DECODE ERROR (Abnormal decoding)** As this is a decoding error code for MP3 format, it is of no relevance to reading of data in CD-DA format, which does not need decoding. As the MP3 decoding process precedes the process of writing in the buffer, this error code is associated with the process that precedes the process with which E-8303 is associated. This code may also be indicated when the quality of the RF signal is deteriorated.				
Player		Measure the error rate in Player Operation mode of Service mode. To which the cause is attributed, disc or player, must be judged first. For measuring, play back the lead-in point indicated in the error code by listening the sound.		
E-8305 **DATA FORMAT ERROR (Abnormal data format)** The CD is played back in a format other than MP3. Or the quality of the RF signal is deteriorated. The data on this symptom are not stored in the internal memory.				
		❶ Check if the CD being played back is in MP3 format.		
Player		❷ Measure the error rate in Player Operation mode of Service mode. To which the cause is attributed, disc or player, must be judged first. For measuring, play back the lead-in point indicated in the error code by listening the sound.	Follow the procedures described in "The error rate measured in Test Operation mode of Service mode is high."	
E-8709 **COMMUNICATION ERROR** See "E8709" error.				
E-9101 **MECHANICAL TIME OUT** • E910190: Abnormality in the disc-loading mechanism (timeout)				
Player			Follow the procedures described in "The error rate measured in Test Operation mode of Service mode is high."	

FAILURE JUDGMENT OF THE Pickup Assy

Item	Specifications	Measurement procedures	Failure judgment	Remarks
Laser Diode (LD) current	Typ 70 mA Max 80 mA	① Make sure that no CD is loaded. ② Enter Service mode. ③ During Test Operation mode, press the TEMPO button to turn the LD on. ④ Measure the voltage difference (DC value) between the Test Lands LD3S and LDCHECK on the MAIN Assy.	If the measurement result of the LD current is 80 mA or more, the LD is deteriorated. **Note:** Check the mounting status of R101 to R104 (22 ohms).	To prevent damage to the LD, after the LD is turned on (Step 3 of the measurement procedures and after), never connect or disconnect the measuring equipment.
Focus coil resistance	3.4 ± 0.5 Ω	① Make sure that no CD is loaded. ② Remove the bottom plate and set the LD short-circuit switch (S1101) to Short-circuiting. ③ Disconnect the FFC cable that connects the RLYB Assy and the MAIN Assy from the CN101 connector. ④ Measure the conductor resistance of the terminal assembly between Pins 13 and 14 of the FFC cable.	If the measurement result is beyond the specified value, the pickup is in failure.	 LD short-circuit switch  Focus coil and Tracking coil
Tracking coil resistance	4.1 ± 0.6 Ω	① Make sure that no CD is loaded. ② Remove the bottom plate and set the LD short-circuit switch (S1101) to Short-circuiting. ③ Disconnect the FFC cable that connects the RLYB Assy and the MAIN Assy from the CN101 connector. ④ Measure the conductor resistance of the terminal assembly between Pins 15 and 16 of the FFC cable.	If the measurement result is beyond the specified value, the pickup is in failure.	
S-curve level Usually use a pressed CD, as the measurement result depends on the disc type.	Reference: 1.5 Vp-p	① Enter Service mode. ② Load a pressed CD. (Standby) ③ During Test Operation mode, press the TIME, A, then CUE buttons to send a command.	The pickup or the MAIN Assy is in failure if the measurement result is more than double or less than 50% of the specified (reference) value.	
Tracking Error (TE) level Usually use a pressed CD, as the measurement result depends on the disc type.	Reference: 1.1 Vp-p	① Enter Service mode. ② Load a pressed CD. (Standby) ③ During Test Operation mode, press the buttons in the following order to send a command: TIME, TEMPO, RELOOP, then LOOPIN twice. ④ Measure the peak-to-peak TE waveform at the TE Test Land on the MAIN Assy.	The pickup or the MAIN Assy is in failure if the measurement result is more than double or less than 50% of the specified (reference) value.	
RFO level Usually use a pressed CD, as the measurement result depends on the disc type.	Reference: 1.2 Vp-p	① Play back a pressed CD. ② Measure the peak-to-peak RF waveform at the RFO Test Land on the MAIN Assy.	The pickup or the MAIN Assy is in failure if the measurement result is more than double or less than 50% of the specified (reference) value.	You may disconnect the measuring equipment during measurement, if you wish.
Auto Gain Control (AGC) RF level The measurement result does not depend on the disc type.	1.2 Vp-p ± 10 %	① Play back a CD. ② During playback, measure the peak-to-peak RF waveform at the AGCRF Test Land on the MAIN Assy.	If the RFO level is within the specified values, and if the AGC RF level is outside the range of the specified values, the MAIN Assy is in failure.	You may disconnect the measuring equipment during measurement, if you wish.

7.1.4 POWER ON SEQUENCE

■ POWER ON SEQUENCE

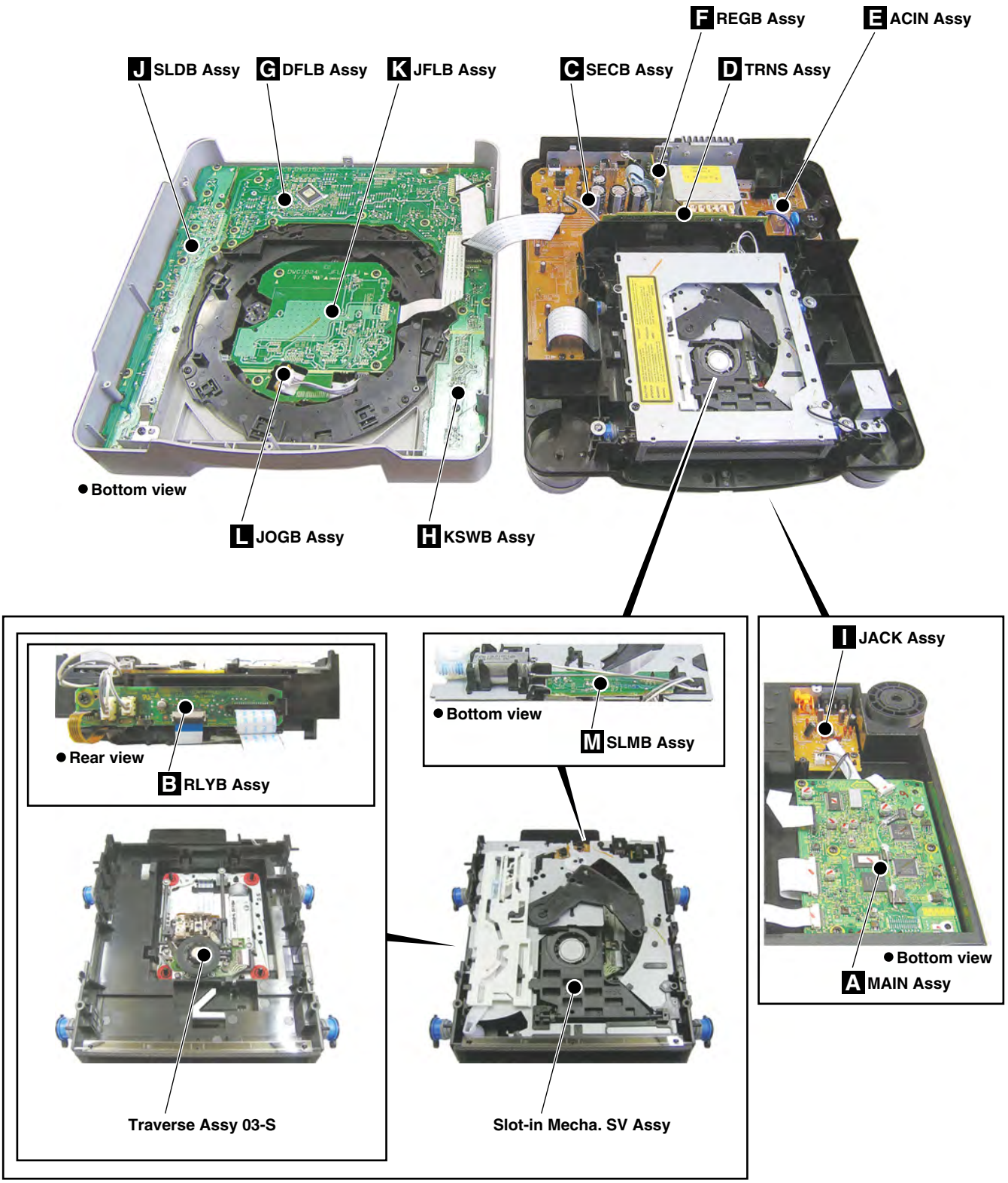

POWER ON
RESET ROOT 1
RESET ROOT 2
DATA-FL/JOG-FL Indication
RESET IC
IC304 (Reset IC) RESET START
IC502 (Reset IC) RESET START
RESET IC
MPU
IC301(MPU) Reset receiving pin P12
IC501(DISPLAY-MPU) Reset receiving pin 12
FPGA
IC302(FPGA) Reset receiving pin 72
IC501(DISPLAY-MPU) Indication 'POWER ON'
'POWERON' data is inside of DISPLAY-MPU.
DISPLAY MPU
IC501(DISPLAY-MPU) Communication start to MPU
DSP
IC701(DSP) Reset receiving pin 47
IC701(DSP) Program download
ServoDSP
IC101 (Servo DSP) Reset receiving pin 90
CD-DRIVE
Inside SW check
Laser Diode ON
LD : Laser Diode
Tracking and focus offset adjustment
Spindle kick & focus sweep & focus on
When a check fails one times,S-curve waveform is measured in RF gain up.
Focus OK check
When S-curve waveform level is 0.88Vp-p or less,focus on is carried out by OEIC and RG gain up.
Spindle acceleration 100msec
When a check fails three times,display EJECT.
EJECT
CLV servo ON
Wait for 300msec
Tracking balance adjustment (T open)
Tracking close
GFS check
GFS : RF LOCK
Focus balance adjusutment
Focus gain adjusutment
Tracking gain adjusutment
RF gain adjusutment
When TOC read is completion
TOC read
The 1st time carries out TOC position memory by stepper accuracy after power on.
If it is a program area, it jump-backs to TOC area.
Search the first tune
Play (mute off)
POWER ON
(No Display)

As CD-DRIVE is same as CDJ-200, CDJ-800MK2' Function is as same it too.

7.1.5 DISASSEMBLY

Note 1: Do NOT look directly into the pickup lens. The laser beam may cause eye injury.
Note 2: Even if the unit shown in the photos and illustrations in this manual may differ from your product, the procedures described here are common.

PCB Location



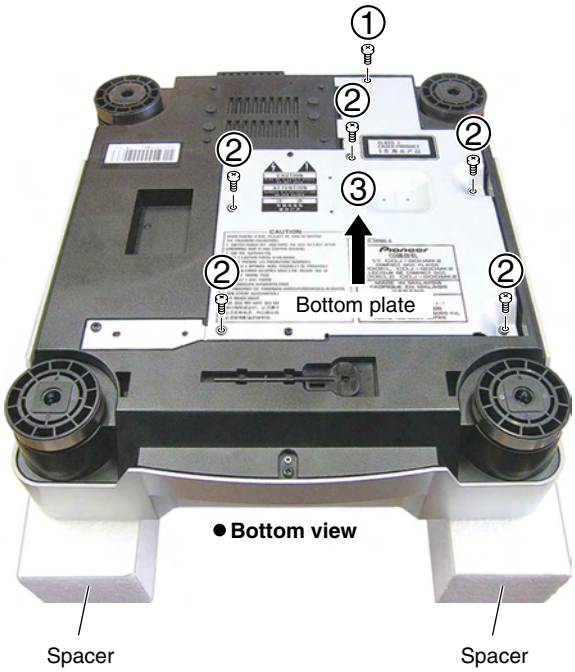
Diagnosis of MAIN Assy

Note: To work on the unit having it set upside-down, place spacers below it, as shown in the photo below, to avoid imparting stress to the sheet SW of the JOG section.

① Remove the one screw.

② Remove the five screws.

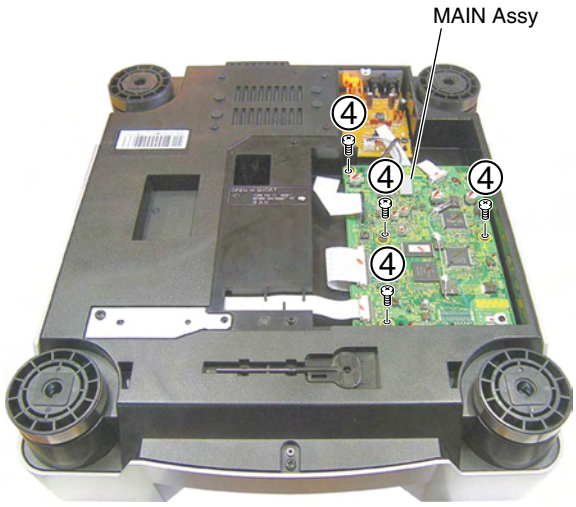
③ Remove the bottom plate.



● **Bottom view**

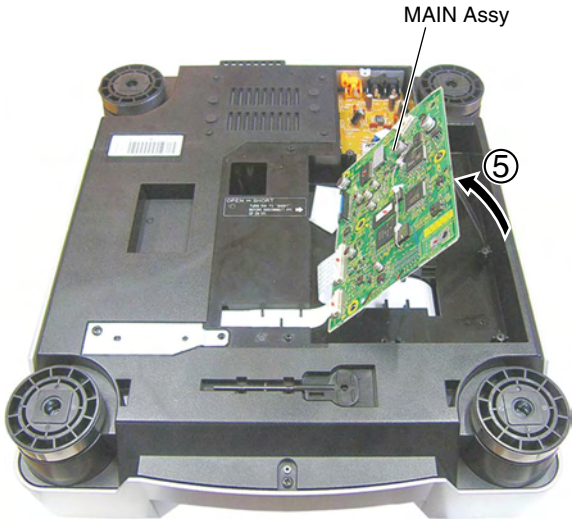
Spacer Spacer

④ Remove the four screws.



● **Bottom view**

⑤ Stand the MAIN Assy.

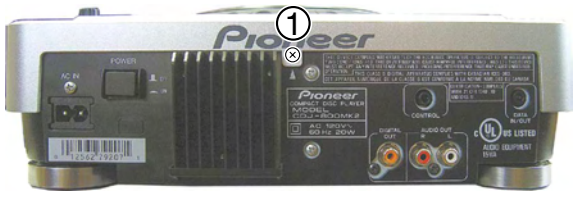


● **Bottom view**

Diagnosis

1 Control Panel Section

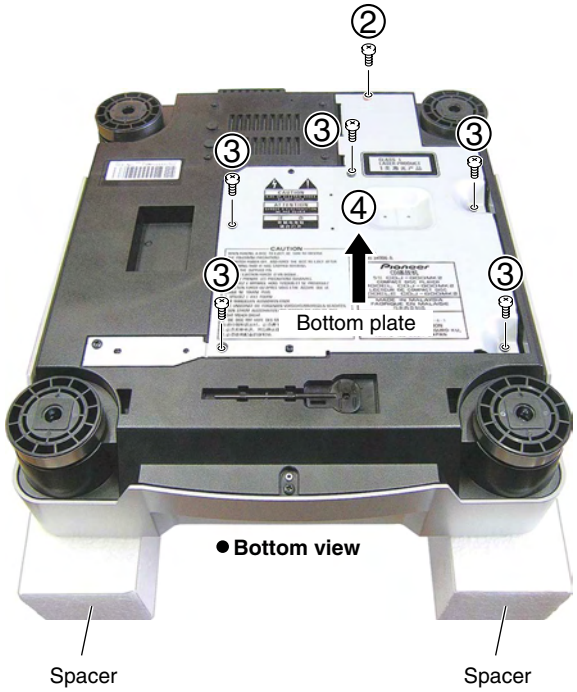
① Remove the one screw.



● Rear view

Note: To work on the unit having it set upside-down, place spacers below it, as shown in the photo below, to avoid imparting stress to the sheet SW of the JOG section.

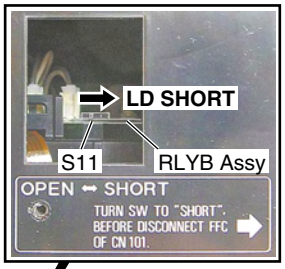
② Remove the one screw.
③ Remove the five screws.
④ Remove the bottom plate.



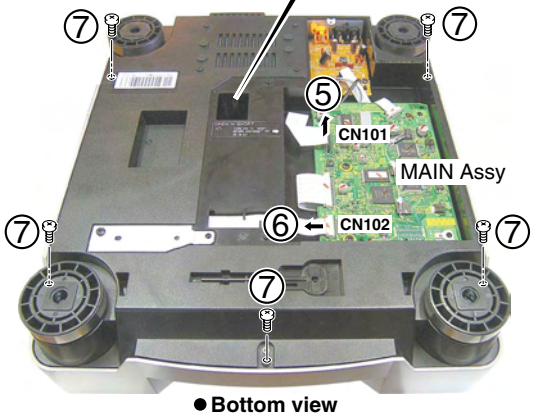
● Bottom view

● Short-circuit switch for the pickup

Before disconnecting the flexible cable for the pickup, change the position of the S1101 switch on the RLYB Assy to LD SHORT.

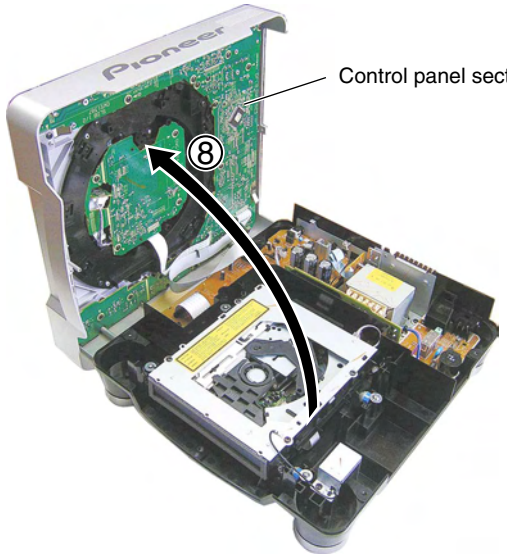


⑤ Disconnect the flexible cable for the pickup.
⑥ Disconnect the flexible cable.
⑦ Remove the five screws.



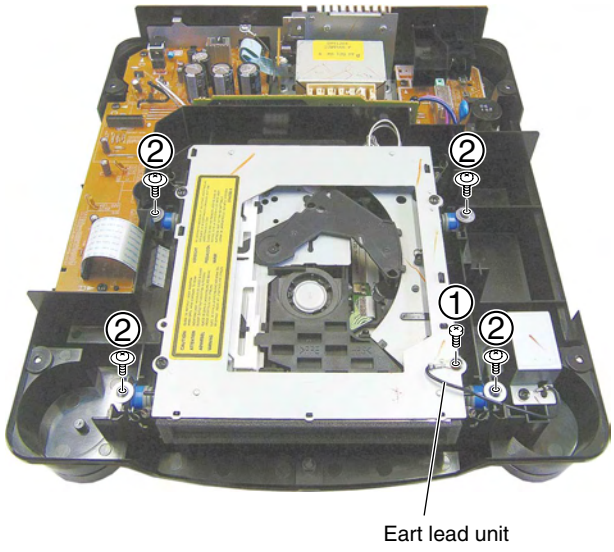
● Bottom view

⑧ Remove the control panel section.

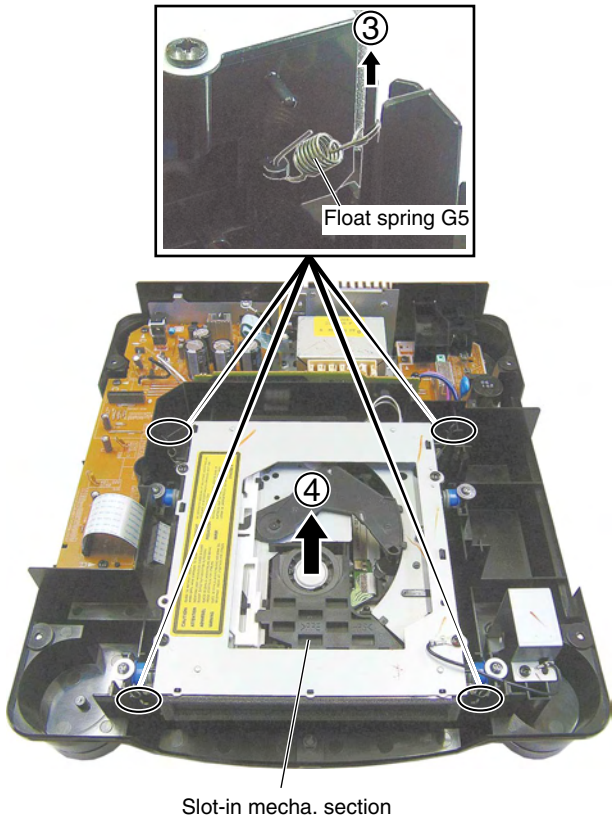


2 Slot-in Mecha. Section

① Remove the earth lead unit by removing the one screw.
② Remove the four DM screws.

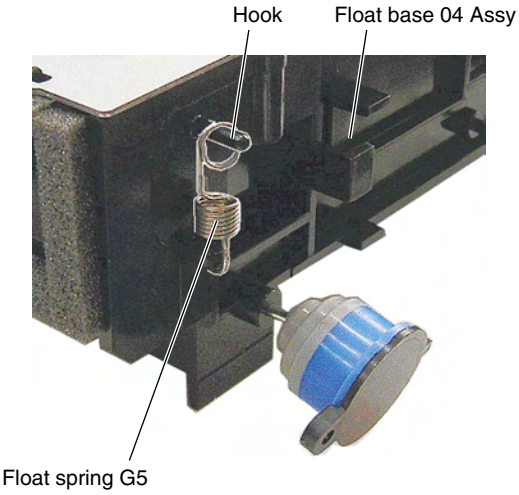


③ Remove the four float springs G5.
④ Remove the slot-in mecha. section.



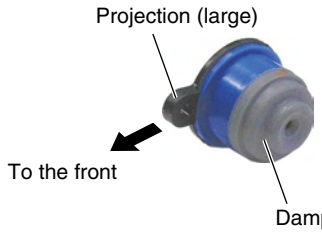
● How to handle the float spring G5

To avoid losing the float spring G5, after removing it, put it on the hook of the float base 04 Assy.



● Direction of the dampers when attaching them

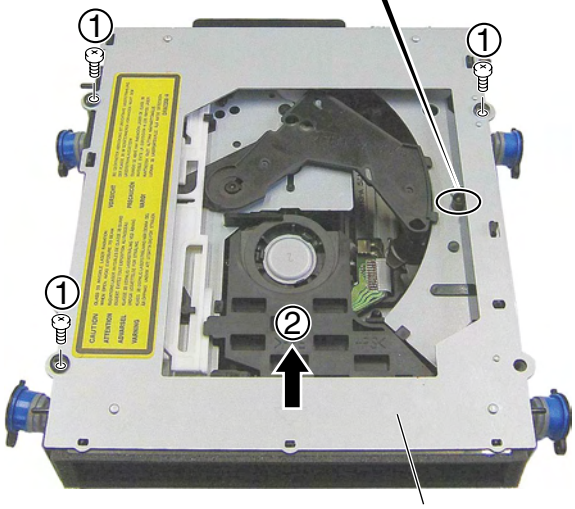
When attaching the dampers, place them so that their projections (large) face front.



3 Slot-in Mecha. SV Assy

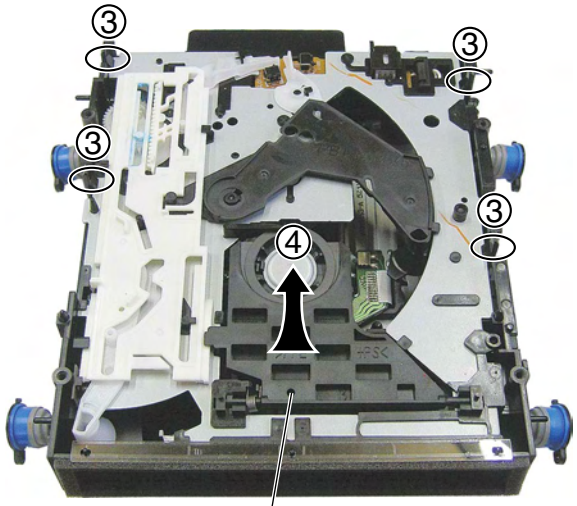
① Remove the three screws.
② Remove the mecha. plate.

Caution:
Be careful not to lost earth spring.



Mecha. plate

③ Unhook the four hooks.
④ Remove the slot-in mecha. SV Assy.

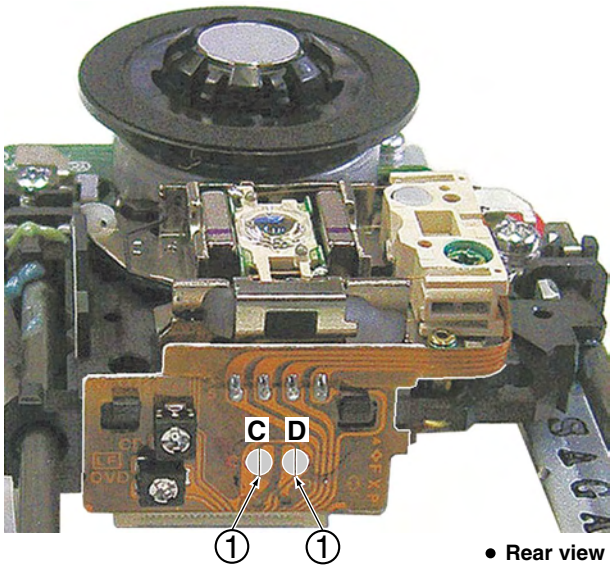


Slot-in mecha. SV Assy

4 Traverse Assy 03-S

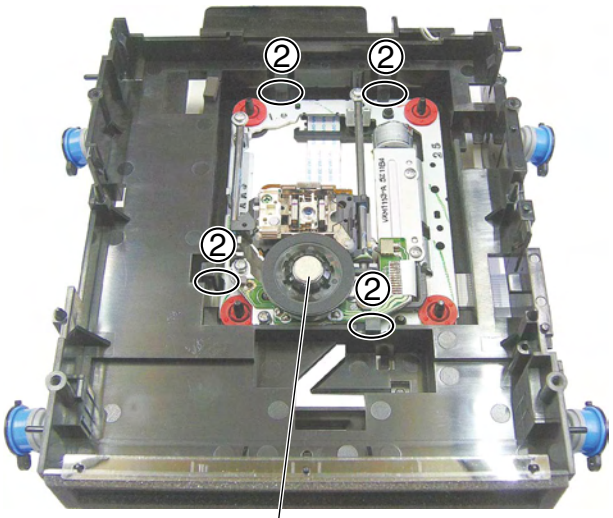
① Short-circuit two points C and D soldering.

Note: After replacement, connect the flexible cable, then remove the soldered joint (open).



● **Rear view**

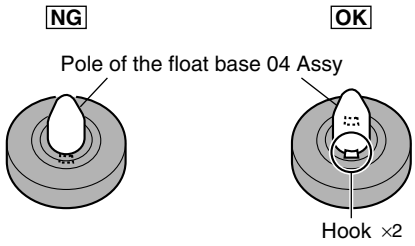
② Unhook the four hooks.
③ Disconnect cables, as required.
④ Remove the traverse Assy 03-S.



Traverse Assy 03-S

Replace

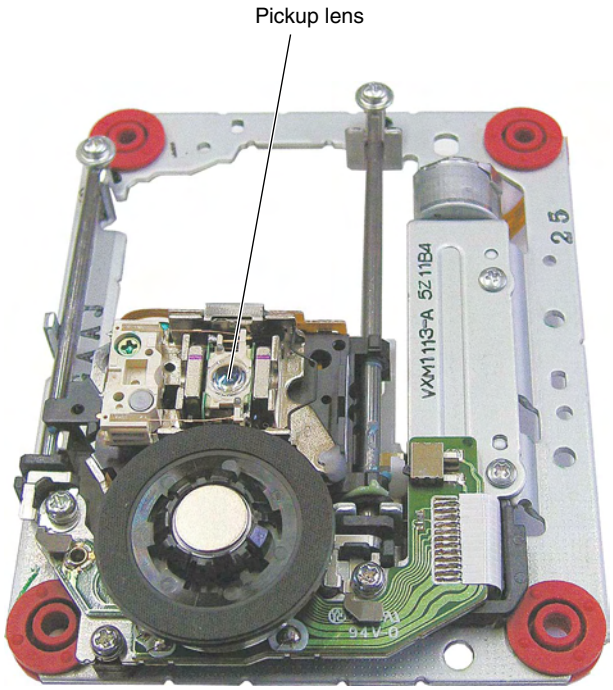
● Note on the float rubber installation



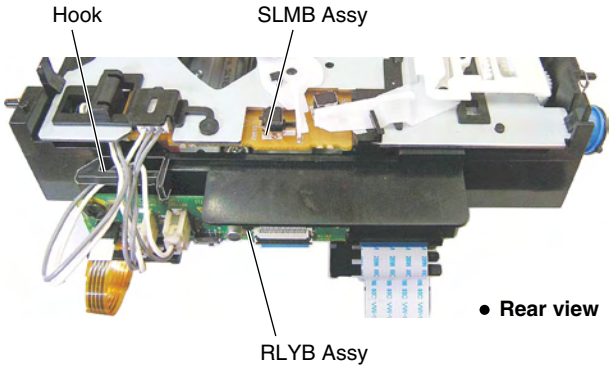
● Cleaning the pickup lens

Before shipment, be sure to clean the pickup lens, using the following cleaning materials:

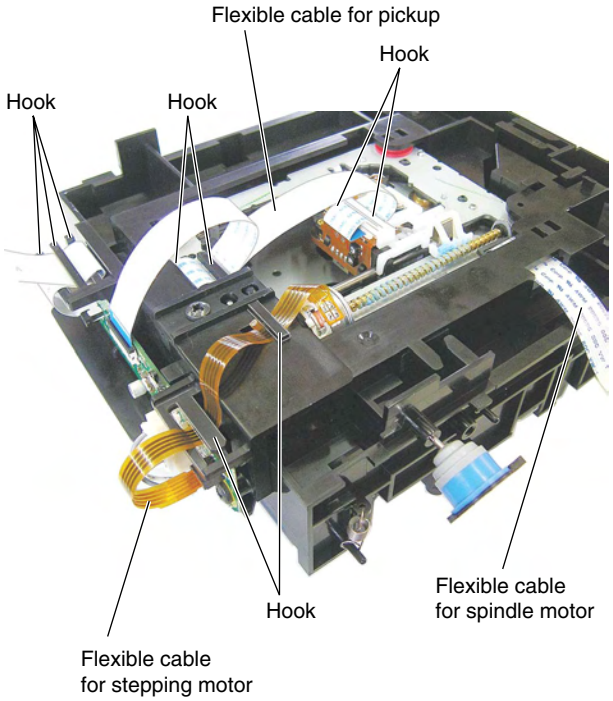
Cleaning liquid : GEM1004
Cleaning paper : GED-008



● Arrangement of the flexible cables



● **Rear view**

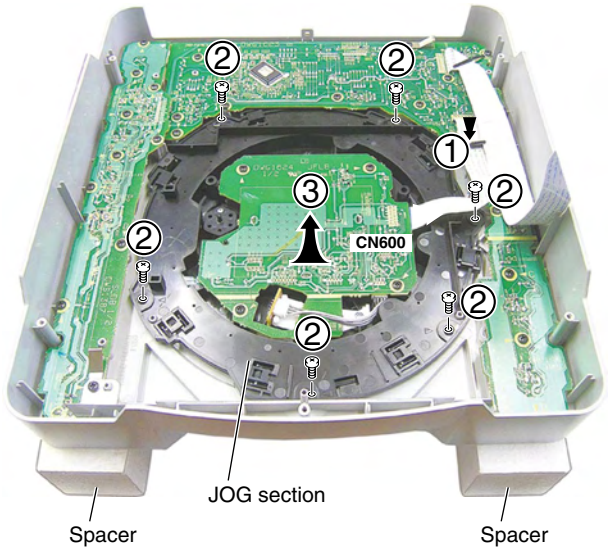


● **Rear / Bottom view**

5 JOG Section

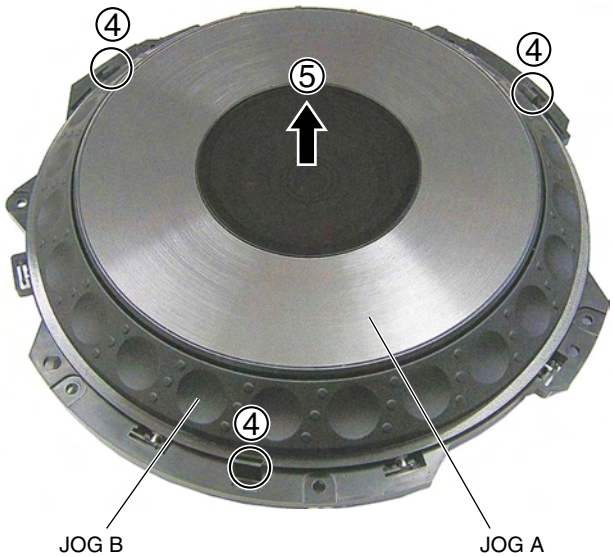
Note: To work on the unit having it set upside-down, place spacers below it, as shown in the photo below, to avoid imparting stress to the sheet SW of the JOG section.

① Disconnect the flexible cable.
② Remove the six screws.
③ Remove the JOG section.



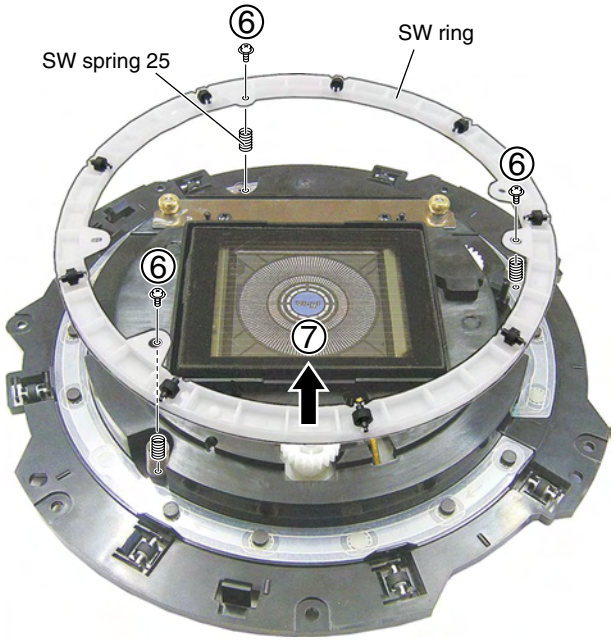
● **Bottom view**

④ Unhook the three hooks.
⑤ Remove the JOG A and JOG Bs.

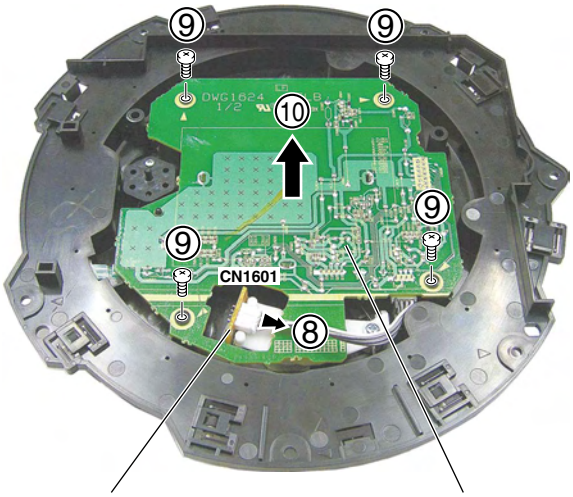


⑥ Remove the three screws.
⑦ Remove the SW ring.

Caution:
Be careful not to lost SW spring 25.

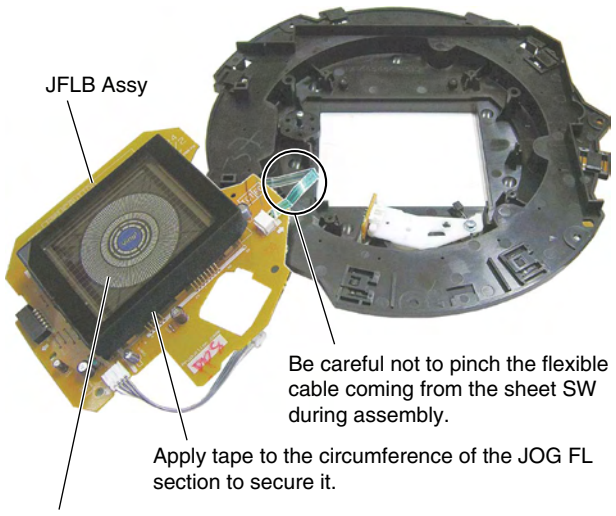


⑧ Disconnect the connector.
⑨ Remove the four screws.
⑩ Remove the JFLB Assy.

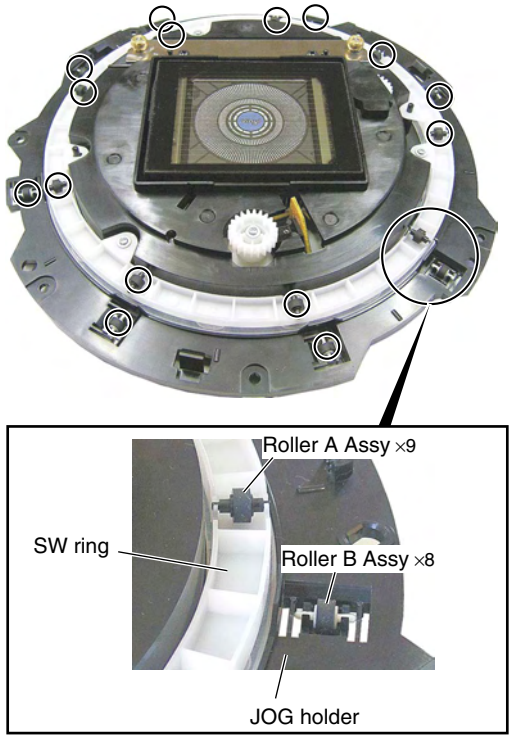


Notes on Replacement

Notes on replacing the JFLB Assy


JFLB Assy
Be careful not to pinch the flexible cable coming from the sheet SW during assembly.
Apply tape to the circumference of the JOG FL section to secure it.
Adhere a reinforcing polycarbonate sheet to the surface.

Places to Roller Assys A and B

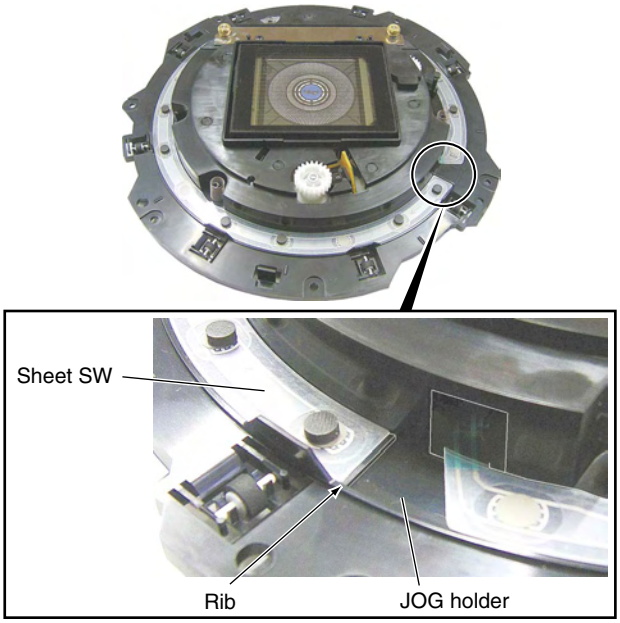


Notes on replacing the Sheet SW

● Place to adhere the Sheet SW

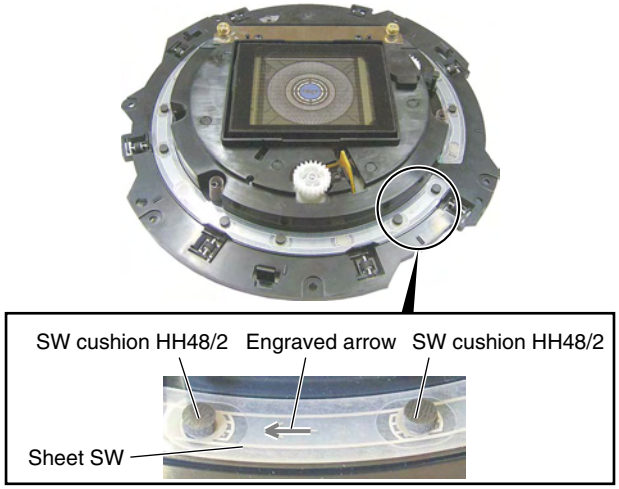
Notes:

1. Be careful not to warp the sheet SW.
2. Remove any dirt on the JOG holder to which the sheet SW is to be adhered. If some adhesive for the old sheet SW remains on the JOG holder, completely remove it with a cloth moistened with alcohol.
3. Do NOT place the sheet SW so that it is mounted on the rib of JOG holder.
4. When adhering the sheet SW, be careful not to trap air bubbles in it. If air bubbles are formed, remove the sheet SW and adhere a new sheet SW.
   Do NOT reuse the removed sheet SW.
5. When making a connection, be sure to first release the lock of the connector then securely relock the connector after making the connection.



● Place to adhere the SW cushions HH48/2

Adhere the cushions to the right and left of the engraved arrows (←) (12 positions in total) on the sheet SW.



7.2 PARTS
7.2.1 IC

• The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

● List of IC

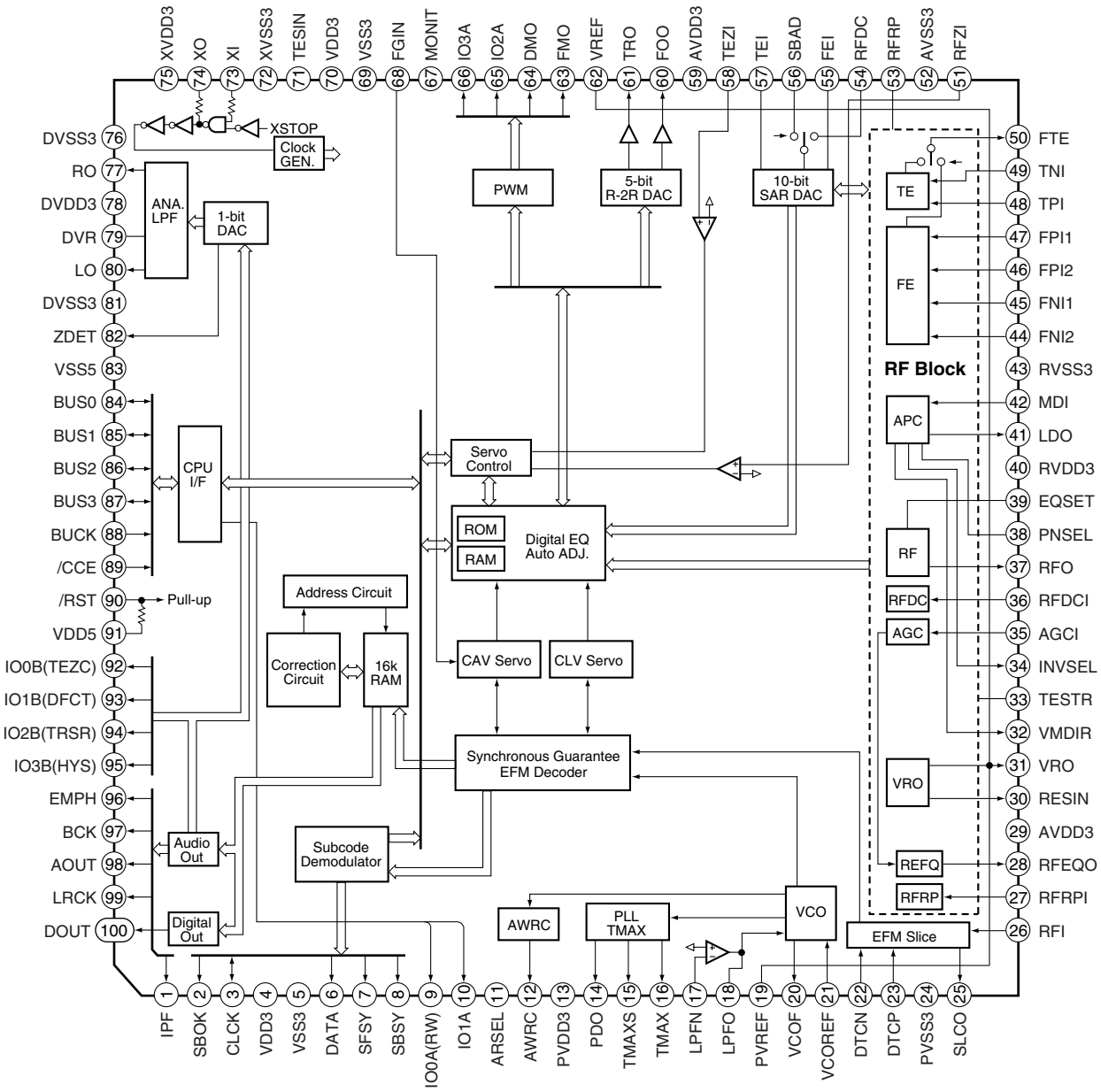
TC94A15FG, PEG237B, DYW1753, SCF5249VM140, BA00BCOWCP-V5, NJM2374AM,TC7S04FU, M63018FP
BA50BC0WFP, NJM4558DX, XC3S50-4VQ100C, K4S641632K-UC75, BU4230G, DSPC56371AF180, PE8001A

■ TC94A15FG (MAIN ASSY : IC101)

• Digital Servo IC

● Pin Assignment (Top view)

● Block Diagram



● Pin Function

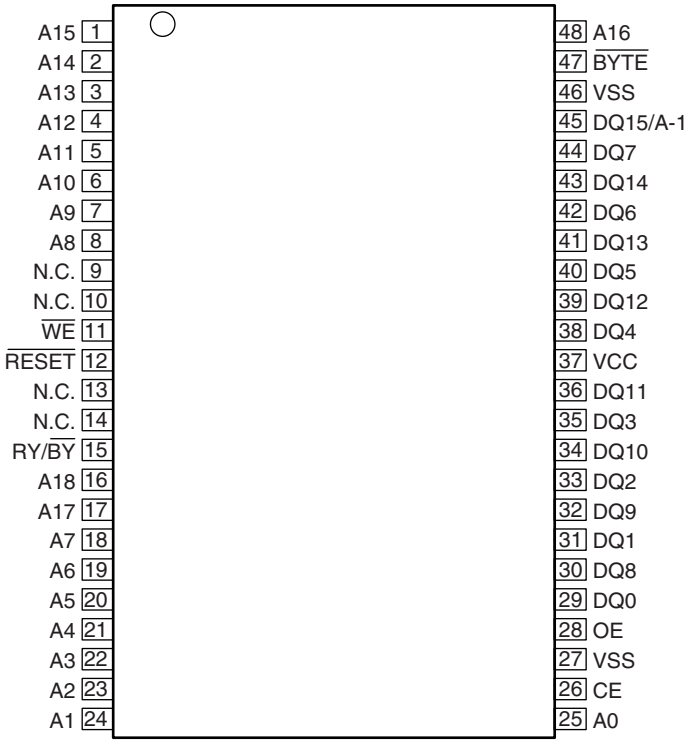
No.	Pin Name	I/O	Pin Function
1	IPF	O	Correction flag output. "H" if the AOUT output is an uncorrectable symbol in C2 correction.
2	SBOK	O	CRCC check result output for subcode Q data. "H" if the check result is OK.
3	CLCK	I/O	Clock input/output for reading subcode P to W data. The polarity of the input/output can be selected with a command.
4	VDD3	–	Power supply for 3.3V digital circuits.
5	VSS3	–	Grounding for digital circuits.
6	DATA	O	Subcode P to W data output.
7	SFSY	O	Playback section frame sync signal output.
8	SBSY	I/O	Subcode block sync output. "H" in the S1 position when a subcode sync is detected.
9	IO0A (RW)	O	"H" when the CD-RW is detected (usually "L"), and switch the OEIC gain.
10	IO1A	O	Unsetting. Always "L"
11	ARSEL	I	Usually fixed at "H" level.
12	AWRC	O	VCO control for active wide-range PLL.
13	PVDD3	–	3.3V power supply dedicated to the PLL section.
14	PDO	O	Signal output for phase difference between EFM and PLCK signals.
15	TMAXS	O	TMAX detection result output. The same signal is output from the TMAX and TMAXS pins.
16	TMAX	O	TMAX detection result output. The same signal is output from the TMAX and TMAXS pins.
17	LPFN	I	Inversion input for PLL section low-pass filter amplifier.
18	LPFO	O	Output for PLL section low-pass filter amplifier.
19	PVREF	–	1.65V reference voltage dedicated to the PLL section.
20	VCOF	O	VCO filter pin.
21	VCOREF	I	Input for VCO center frequency reference level.
22	DTCN	O	Analog slicer filter.
23	DTCP	O	Analog slicer filter.
24	PVSS3	–	Grounding dedicated to the PLL section.
25	SLCO	I	EFM slice level output.
26	RFI	I	RF signal input. An input resistance can be selected using a command.
27	RFRPI	I	RF ripple signal input.
28	RFEQO	O	RF equalizer circuit output.
29	AVDD3	–	Power supply for 3.3V analog circuits.
30	RESIN	I	Pin for connecting a rtesistor for reference current generation.
31	VRO	O	1.65V reference voltage output.
32	VMDIR	–	1.533V reference voltage output.
33	TESTR	O	Pin for connecting filter for RFEQO offset correction.
34	INVSEL	I	Test pin, usually fixed at "L" level.
35	AGCI	I	Input for RF signal amplitude adjustment amp.
36	RFDCI	I	Input for RF signal peak detection.
37	RFO	O	Output for RF signal generation amp.
38	PNSEL	I	Test pin, usually fixed at "H" level.
39	EQSET	O	External-connection for RF signal equalizer.
40	RVDD3	–	Power supply for 3.3V RF amp. core section.
41	LDO	O	Laser diode amp. output.
42	MDI	I	Monitor photodiode amp. input.
43	RVSS3	–	Grounding for 3.3V RF amp. core section.
44	FNI2	I	Main beam input. To be connected to PIN diode C.
45	FNI1	I	Main beam input. To be connected to PIN diode A.
46	FPI2	I	Main beam input. To be connected to PIN diode D.
47	FPI1	I	Main beam input. To be connected to PIN diode B.
48	TPI	I	Subbeam input. To be connected to PIN diode F.
49	FNI	I	Subbeam input. To be connected to PIN diode E.

No.	Pin Name	I/O	Pin Function
50	FTE	O	Focus/tracking signal output. (Test pin for servo characteristiv measurement.)
51	RFZI	I	Input for RF ripple zero-cross signal.
52	AVSS3	–	Grounding for analog circuits.
53	RFRP	O	RF ripple signal output.
54	RFDC	O	Pin for the RF peak detection signal supporting hologram.
55	FEI	O	Focus error signal pin.
56	SBAD	O	Subbeam addition signal pin.
57	TEI	O	Tracking error signal pin.
58	TEZI	I	Input for tracking error signal zero-cross.
59	AVDD3	–	Power supply for 3.3V analog circuits.
60	FOO	O	Focus equalizer output.
61	TRO	O	Tracking equalizer output.
62	VREF	O	Reference voltage for analog circuits.
63	FMO	O	Speed error/feed equalizer output.
64	DMO	O	Disc equalizer output.
65	IO2A	O	Unsetting. Always "L"
66	IO3A	O	Unsetting. Always "L"
67	MONIT	O	Pin for monitoring signals in the DSP.
68	FGIN	I	FG signal input for CAV. CLV: "L", CAV: FG input
69	VSS3	–	Grounding for digital circuits.
70	VDD3	–	Power supply for 3.3V digital circuits.
71	TESIN	I	Test input pin, usually fixed at "L" level.
72	XVSS3	–	Grounding for system clock oscillator circuit.
73	XI	I	Input for system clock oscillator circuit.
74	XO	O	Output for system clock oscillator circuit.
75	XVDD3	–	Power supply for 3.3V system clock oscillator circuit.
76	DVSS3	–	Grounding for 1-bit DAC.
77	RO	O	R channel data normal output for 1-bit DAC.
78	DVDD3	–	3.3V power supply for 1-bit DAC.
79	DVR	O	Reference voltage for 1-bit DAC.
80	LO	O	L channel data normal output for 1-bit DAC.
81	DVSS3	–	Grounding for 1-bit DAC.
82	ZDET	O	Zero detection flag output for 1-bit DAC.
83	VSS5	–	Grounding for interface.
84	BUS0	I/O	Data input/output for the microcomputer interface
85	BUS1	I/O	Data input/output for the microcomputer interface
86	BUS2	I/O	Data input/output for the microcomputer interface
87	BUS3	I/O	Data input/output for the microcomputer interface
88	BUCK	I	Clock input for the microcomputer interface
89	/CCE	I	Chip enable signal input for the microcontroller interface. BUS3 to BUS0 are active if this pin is "L".
90	/RST	I	Reset signal input. The internal registers and servo section registers are reset, respectively, when the reset signal is "L" and on the rising edge of the reset signal.
91	VDD5	–	Power supply for the interface,
92	IO0B (TEZC)	O	The signal that inverts H/L with TE zero-cross.
93	IO1B (DFCT)	O	Defect signal. Normally "H", but it becomes "L" when detecting dirts on the disc.
94	IO2B (TRSR)	O	It becomes "L" during tracking close or search.
95	IO3B (HYS)	O	It becomes "L" in the hysteresis operation.
96	EMPH	O	Emphasis flag output. EMPH ON: "H", EMPH OFF: "L" The output polarity is switched, using a command.
97	BCK	O	Bit clock output. 32fs, 48fs and 64fs are selected, using a command.
98	AOUT	O	Audio data output. Which bit is first (MSB first or LSB first) can be selected, using a command.
99	LRCK	O	LR channel clock output. L ch: "L", R ch: "H" The output polarity can be inverted, using a command.
100	DOUT	O	Digital-out output

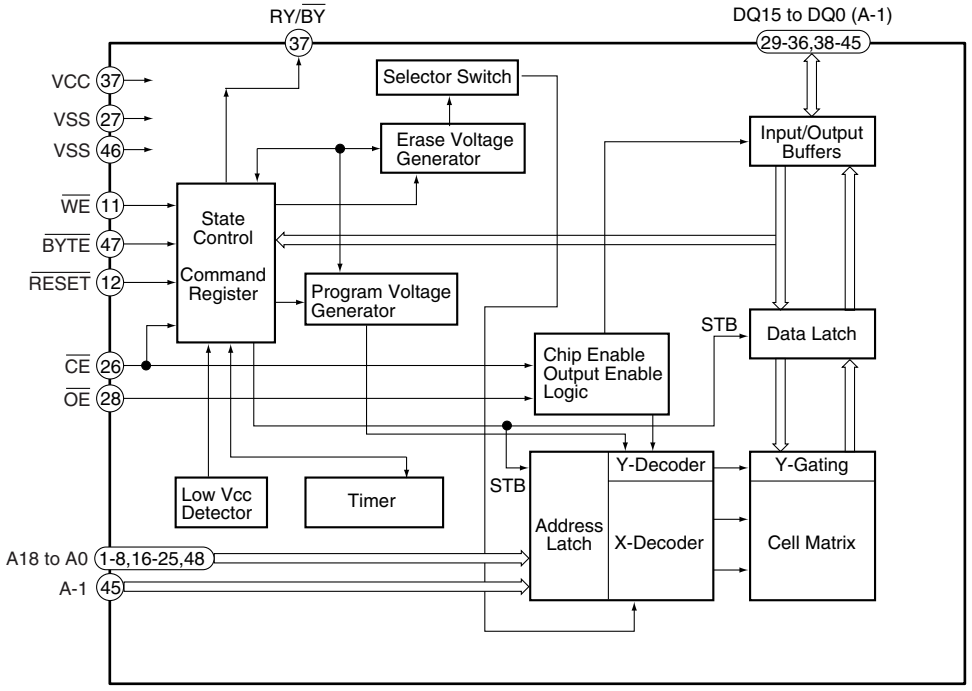
■ DYW1753 (MAIN ASSY : IC300)

• Flash ROM

● Pin Arrangement (Top view)



● Block Diagram



● **Pin Function**

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
1	A15	I	Address input	25	A0	I	Address input
2	A14	I	Address input	26	$\overline{CE}$	I	Chip enable
3	A13	I	Address input	27	VSS	–	Ground
4	A12	I	Address input	28	$\overline{OE}$	I	Output enable
5	A11	I	Address input	29	DQ0	I/O	Data input/output
6	A10	I	Address input	30	DQ8	I/O	Data input/output
7	A9	I	Address input	31	DQ1	I/O	Data input/output
8	A8	I	Address input	32	DQ9	I/O	Data input/output
9	N.C.	–	No connection	33	DQ2	I/O	Data input/output
10	N.C.	–	No connection	34	DQ10	I/O	Data input/output
11	$\overline{WE}$	I	Write enable	35	DQ3	I/O	Data input/output
12	$\overline{RESET}$	I	Hardware reset	36	DQ11	I/O	Data input/output
13	N.C.	–	No connection	37	VCC	–	Power supply
14	N.C.	–	No connection	38	DQ4	I/O	Data input/output
15	RY/$\overline{BY}$	O	Ready/Busy output	39	DQ12	I/O	Data input/output
16	A18	I	Address input	40	DQ5	I/O	Data input/output
17	A17	I	Address input	41	DQ13	I/O	Data input/output
18	A7	I	Address input	42	DQ6	I/O	Data input/output
19	A6	I	Address input	43	DQ14	I/O	Data input/output
20	A5	I	Address input	44	DQ7	I/O	Data input/output
21	A4	I	Address input	45	DQ15/A-1	I/O	Data input/output / Address input
22	A3	I	Address input	46	VSS	–	Ground
23	A2	I	Address input	47	$\overline{BYTE}$	I	Selects 8-bit or 16-bit mode
24	A1	I	Address input	48	A16	I	Address input

■ SCF5249LAG140 (MAIN ASSY : IC301)

• 32-bit RISC MPU

● Block Diagram

SCF5249 Block Diagram

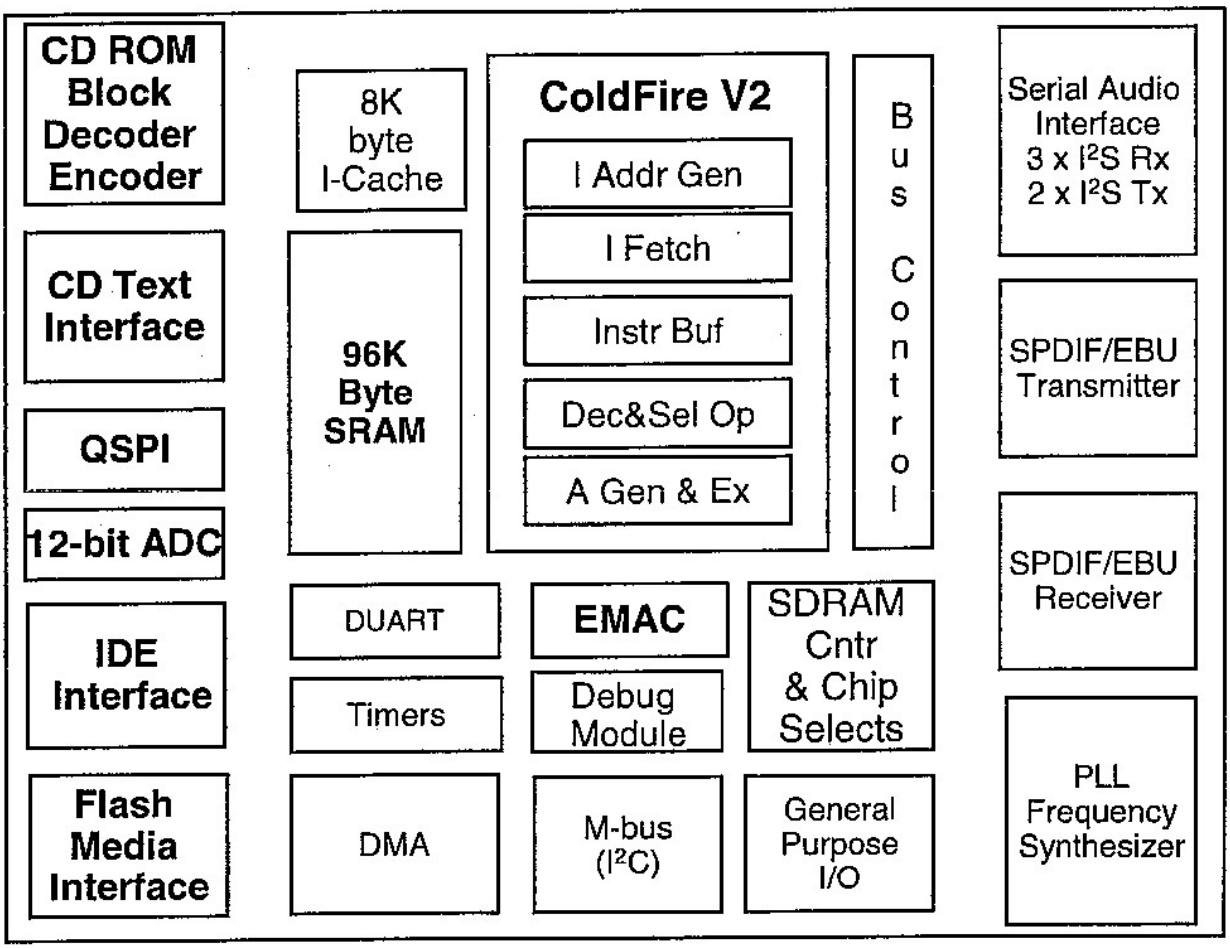


Figure 1. SCF5249 Block Diagram

IC301 : SCF5249VM140 _No.1/4

● **Pin Function**

No.	Pin Name	I/O	Pin Function
D4	SCL/QSPI_CLK	I/O	IIC clock/QSPI clock pin function select is PLLCR(11)
A1	CS0	O	Static chip select 0
D3	A21	O	SDRAM address / static adr
B1	A11	O	SDRAM address / static adr
C2	A10	O	SDRAM address / static adr
C1	A9	O	SDRAM address / static adr
E3	CMD_SDIO2/GPIO34	IO	MemoryStick/SD
D2	A18	O	SDRAM address / static adr
D1	A17	O	SDRAM address / static adr
E2	BCLK/GPIO10	I/O	SDRAM clock output
F3	SCLK_OUT/GPIO15	I/O	MemoryStick/SD
E1	BCLKE	O	SDRAM clock enable output
E4	SDA/QSPI_DIN	I/O	IIC data/QSPI data in function select is PLLCR(11)
F2	DATA24	I/O	Data bus bit 24
G3	A22	O	SDRAM address / static adr
F1	SDUDQM	O	SDRAM UDQM
F4	EF/GPIO19	IO	Error flag input
G4	SDATA0_SDIO1/GPIO54	I/O	MemoryStick/SD
G1	DATA25	I/O	Data bus bit 25
G2	DATA26	I/O	Data bus bit 26
H3	RSTO/SDATA2_BS2	I/O	Reset output/MemoryStick/SD/
H1	DATA27	I/O	Data bus bit 27
H4	PAD-GND	–	PAD-GND
H4	PAD-GND	–	PAD-GND
H2	DATA28	I/O	Data bus bit 28
J1	DATA29	I/O	Data bus bit 29
J3	SDATA3/GPIO56	IO	SD interface data line
J2	DATA30	I/O	Data bus bit 30
J4	BUFENB1/GPIO57	IO	External buffer 1 enable
K1	DATA31	I/O	Data bus bit 31
K6	CORE-VDD	–	CORE-VDD
K6	CORE-VDD	–	CORE-VDD
K2	A13	O	SDRAM address / static adr
K3	A25/GPO8	O	SDRAM address / static adr
K5	CORE-GND	–	CORE-GND
K5	CORE-GND	–	CORE-GND
K4	A 23	O	SDRAM address / static adr
L1	A14	O	SDRAM address / static adr
L2	A15	O	SDRAM address / static adr
M1	A16	O	SDRAM address / static adr
L3	PAD-VDD	–	PAD-VDD
L3	PAD-VDD	–	PAD-VDD
M2	A19	O	SDRAM address / static adr
N1	A20	O	SDRAM address / static adr
L4	QSPI_CS1/GPIO24	IO	QSPI select 1
M3	TEST2	I	Structural test
N2	SDRAM_CS1	O	SDRAM chip select out 1
M4	SDATA1_BS1/GPIO9	I/O	MemoryStick/SD
P1	SDRAS	O	SDRAM RAS
P2	SDCAS	O	SDRAM CAS
N3	SDWE	O	SDRAM write enable
P3	SDLDQM	O	SDRAM LDQM
N4	GPIO5	I/O	General purpose i/o
P4	QSPI_CS0/GPIO29	I/O	QSPI chip select 0
N5	QSPI_DOUT/GPIO26	I/O	Qspsi data out

IC301 : SCF5249VM140_No.2/4

No.	Pin Name	I/O	Pin Function
L5	GPIO6	I/O	General purpose i/o
P5	DATA21	I/O	Data bus bit 21
N6	DATA19	I/O	Data bus bit 19
L6	QSPI_CS2/GPIO21	I/O	QSPI chip select 2
P6	DATA20	I/O	Data bus bit 20
L7	DATA22	I/O	Data bus bit 22
P7	DATA18	I/O	Data bus bit 18
K7	DATA23	I/O	Data bus bit 23
N7	DATA17	I/O	Data bus bit 17
L8	QSPI_CS3/GPIO22	IO	QSPI Chip Select 3
K8	PAD-VDD	–	PAD-VDD
K8	PAD-VDD	–	PAD-VDD
P8	DATA16	I/O	data bus bit 16
N8	SDRAM_CS2/GPIO7	I/O	SDRAM chip select out 2 gpo
P9	EBUOUT2/GPO37	O	Audio interfaces EBU out 2
L9	CFLG/GPIO18	IO	CFLG input
N9	EBUOUT1/GPO36	O	Audio interfaces EBU out 1
K9	CORE-GND	–	CORE-GND
K9	CORE-GND	–	CORE-GND
P10	EBUIN3/ADIN0/GPI38	I	Audio interfaces EBU in 3 A/D convertor input 0
N10	EBUIN2/GPI37	I	Audio interfaces EBU in 2
L10	CORE-VDD	–	CORE-VDD
L10	CORE-VDD	–	CORE-VDD
P11	SCL2/GPIO3	I/O	IIC clock
P12	RSTI	I	Reset input
N11	TOUT1/ADOUT/GPO35	O	Timer output 1/ad output
P13	LRCK2/GPIO44	IO	Audio interfaces serial word clock 2
N12	OE	O	Output Enable
M11	SDA2/GPIO55	I/O	IIC 2 data line
P14	SDATAO2/GPO41	O	Audio interfaces serial data 2 out
N13	SCLK2/GPIO48	IO	Audio interfaces serial clock 2
K10	PAD-GND	–	PAD-GND
K10	PAD-GND	–	PAD-GND
K11	BUFENB2/GPIO17	IO	External buffer 2 enable
M12	TEST3	I	Structural test
L12	SDATAO1/GPIO25	IO	Audio interfaces serial data 1 out
N14	LRCK1	IO	Audio interfaces serial word clock 1
M13	LRCK4/GPIO46	IO	Audio interfaces serial word clock 4
M14	SDATAI4/GPI42	I	Audio interfaces serial data 4 in
L13	SCLK1	IO	Audio interfaces serial clock 1
L14	SCLK4/GPIO50	IO	Audio interfaces serial clock 4
L11	TA/GPIO20	I/O	Transfer Acknowledge
K13	SDATAI1	I	Audio interfaces serial data 1 in
K12	EBUIN1/GPI36	I	Audio interfaces EBU in 1
K14	PLLGRDVDD	IO	PLL guard supply (1.8V)
J11	PLLGRDGND	–	PLL guard supply GND
J13	PLLPADGND	–	3.3 Volt PLL GND
J12	PLLPADVDD	–	3.3 Volt PLL VDD
J14	PLLCOREGND	–	1.8 Volt PLL analog supply-GND
H11	PLLCOREVDD	–	1.8 Volt PLL analog supply-VDD
H12	IDE-DIOW/GPIO14	IO	ide diow
H14	CRIN	I	crystal
H13	IDE-DIOR/GPIO13	IO	IDE DIOR
G11	IDE-IORDY/GPIO16	I/O	IDE IORDY

IC301 : SCF5249VM140_No.3/4

No.	Pin Name	I/O	Pin Function
G11	IDE-IORDY/GPIO16	I/O	IDE IORDY
G14	MCLK1/GPO39	O	Audio master clock output 1
G12	SUBR/GPIO53	IO	Subcode data
G13	MCLK2/GPO42	O	Audio master clock output 2
F14	XTRIM/GPO38	O	Audio interfaces X-tal trim
F11	TRST/DSCLK	I	Jtag
F13	SFSY/GPIO52	IO	Subcode sync
E9	CORE-VDD	–	CORE-VDD
E9	CORE-VDD	–	CORE-VDD
E14	RW_B	O	Bus write enable
F12	RCK/GPIO 51	IO	Subcode clock
E13	TMS/BKPT	I	Jtag
E10	CORE-GND	–	CORE-GND
E10	CORE-GND	–	CORE-GND
E12	TCK	I	Jtag
E11	PAD-GND	–	PAD-GND
E11	PAD-GND	–	PAD-GND
D14	PST3/GPIO 62	IO	ColdFire debug port
D13	CNPSTCLK/GPO 63	O	Coldfire debug clock
C14	PST1/GPIO 60	IO	ColdFire debug port
D12	PAD-VDD	–	PAD-VDD
D12	PAD-VDD	–	PAD-VDD
C13	PST2/GPIO 61	IO	ColdFire debug port
B14	PST0/GPIO 59	IO	ColdFire debug port
D11	TDI/DSI	I	Jtag
C12	TEST0	I	Structural test
B13	TIN0/GPI33	i	Timer input 0
C11	HI-Z	I	Jtag
A14	DDATA 3 / GPIO 4	IO	ColdFire debug port
A13	TOUT0 / GPO33	O	Timer output 0
B12	DDATA1/GPIO 1	IO	ColdFire debug port
A12	DDATA2/GPIO 2	IO	ColdFire debug port
B11	CTS2_B / ADIN3/GP131	I	Second UART clear to send, AD input 3
A11	DDATA0/GPIO 0	IO	ColdFire debug port
B10	RXD2 / GPI28/ADIN2	I	Second UART receive data input AD input 2
D10	TDSO	O	Jtag
A10	RTS2_B/GPO31	O	Second UART request to send
B9	SDATAI3 / GPI 41	I	audio interfaces serial data 3 in
D9	CTS1_B/GPI30	I	First UART clear to send
A9	TXD2/GPO28	O	Second UART transmit data output
D8	RTS1_B / GPO30	O	First UART request to send
A8	EBUIN4/ADIN1/GPI 39	I	audio interfaces EBU in 4/ AD convertor input 1
E8	SRE/GPIO11	IO	SmartMedia read enable
B8	LRCK3 / GPIO 45	IO	Audio interfaces serial word clock 3
E7	SWE/GPI012	IO	SmartMedia write enable
D7	TXD1/GPO27	O	First UART transmit data output
A7	SCLK3/GPIO49	IO	Audio interfaces serial clock 3
B7	RXD1 / GPI27	I	First UART receive data input
A6	CS1 / GPIO58	IO	Static chip select I / gpio I
E6	CORE-GND	–	CORE-GND
E6	CORE-GND	–	CORE-GND
B6	A1	O	Static address A1
D6	TIN1/GP1O23	IO	Timer I in
A5	A2	O	Static address A2

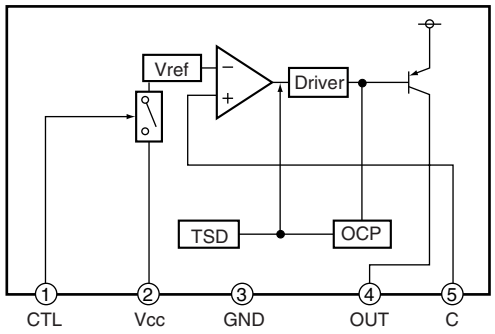
IC301 : SCF5249VM140_No.4/4

No.	Pin Name	I/O	Pin Function
B5	A3	O	Static address A3
D5	PAD-GND	–	PAD-GND
D5	PAD-GND	–	PAD-GND
A4	A4	O	Static adr 4
A3	A6	O	Static adr6
B4	A5	O	Static adr 5
A2	A8	O	Static adr 8
B3	A7	O	Static adr7
C4	CORE-VDD	–	CORE-VDD
C4	CORE-VDD	–	CORE-VDD
B2	A12	O	SDRAM address / static adr
C3	TEST1	I	Structural test
E5	PAD-VDD	–	PAD-VDD
E5	PAD-VDD	–	PAD-VDD

BA00BC0WCP-V5 (SECB ASSY : IC50, REGB ASSY : IC91, IC92)

• Regulator IC (Built-in thermal shutdown protection, output variable type)

● Block Diagram



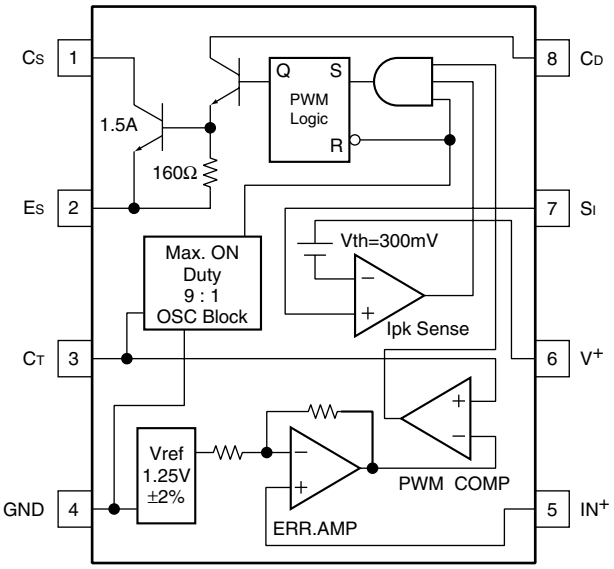
● Pin Function

No.	Pin Name	I/O	Pin Function
1	CTL	I	Output switch control
2	Vcc	–	Power supply
3	GND	–	Ground
4	OUT	O	Output
5	C	I	Voltage comparison

NJM2374AM (SECB ASSY : IC51)

• PWM TYPE DC/DC CONVERTER IC

● Block Diagram



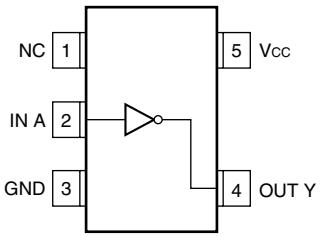
● Pin Function

No.	Pin Name	I/O	Pin Function
1	Cs	I	Collector Terminal
2	Es	O	Emitter Terminal
3	Ct	I	Timing Conndenser Connection
4	GND	–	Ground
5	IN+	I	Reference Voltaage
6	V+	–	Power supply
7	SI	I	Current Detection Terminal
8	CD	I	Logic Control Terminal

TC7S04FU (SECB ASSY : IC52)

• INVERTER IC (Logic IC)

● Block Diagram



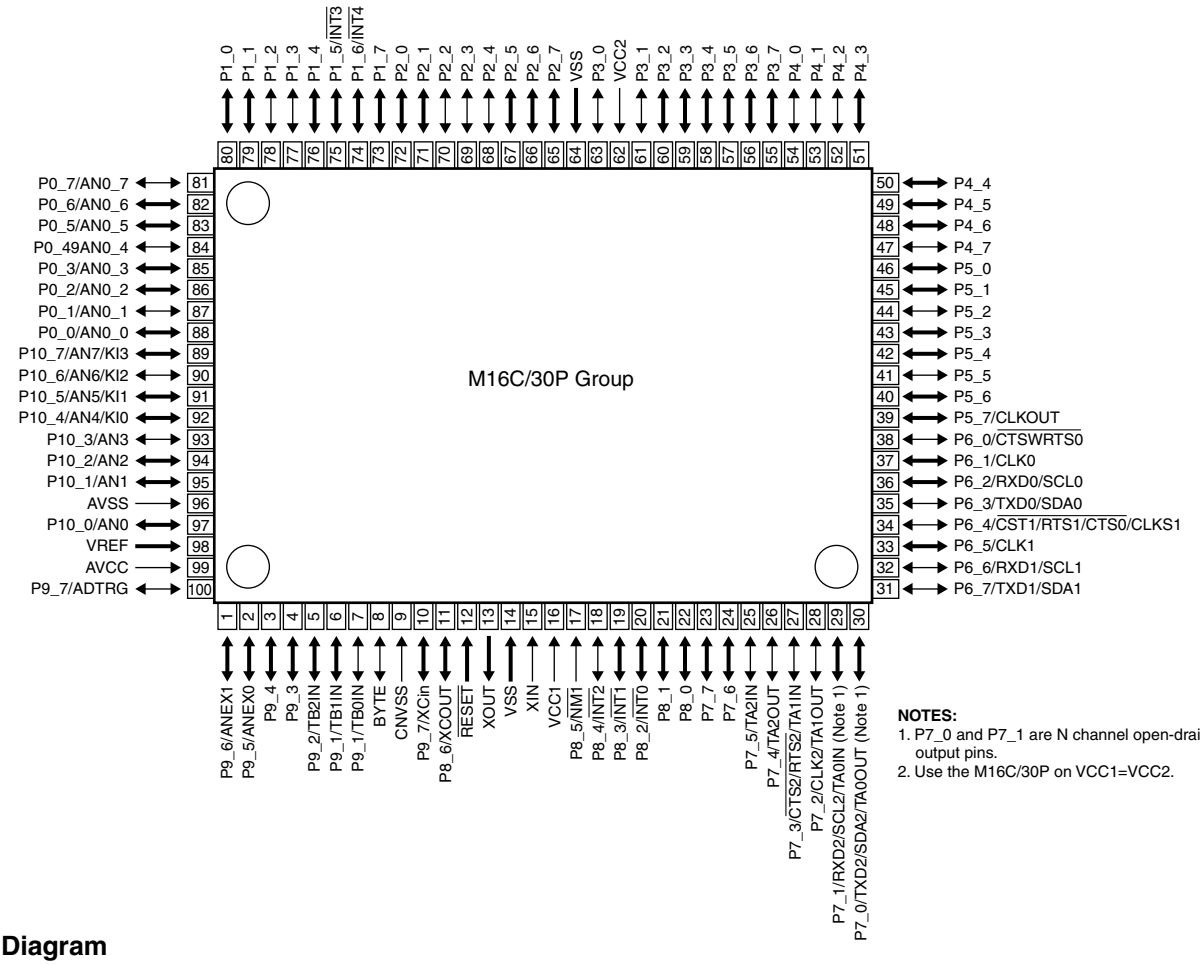
● Pin Function

No.	Pin Name	I/O	Pin Function
1	NC	–	Non connection
2	IN A	I	Input
3	GND	–	Ground
4	OUT Y	0	Output
5	Vcc	–	Power supply

PEG237B (DFLB ASSY : IC501)

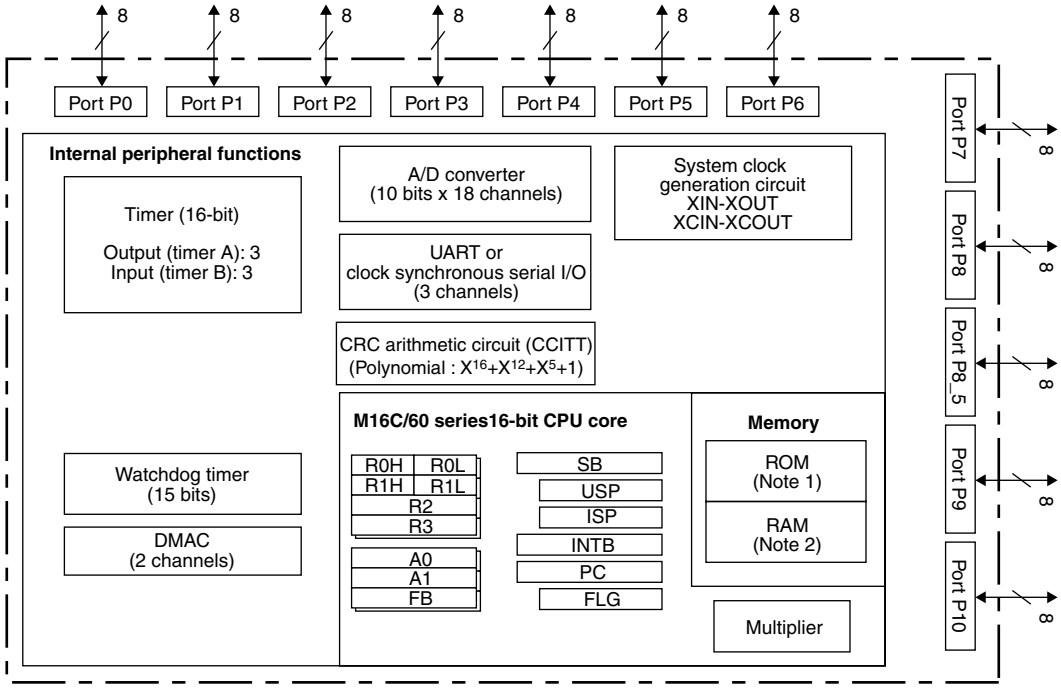
• Display Microcomputer

● Pin Arrangement (Top view)



NOTES:
1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/30P on VCC1=VCC2.

● Block Diagram



(Note 1) ROM size depends on microcomputer type.
(Note 2) RAM size depends on microcomputer type.

● **Pin Function**

No.	Pin Name	I/O	Pin Function
1	–	I	Not used (ground)
2	TCH/REL	I	Volume input (A/D conversion port) For VINYL SPEED ADJUST
3	MODEL2	I	Model setting 2 Distinguish between CDJ-800MK2, CDJ-1000MK3 and DVJ-1000.
4	MODEL1	I	Model setting 1
5	–	O	Not used (non connection)
6	JOG1	I	Pulse period measurement processing
7	–	O	Not used (non connection)
8	–	–	Not used (ground)
9	CNVss	–	For built-in flash memory updating (not used)
10	–	I	Not used (ground)
11	–	I	Not used (ground)
12	XRST	–	Reset input
13	XOUT	–	16 MHz clock input
14	Vss	–	Ground
15	XIN	–	16MHz clock input
16	Vcc	–	Power supply 5 V
17	XNMI	I	
18	–	I	Not used (power supply 5 V)
19	–	I	Not used (power supply 5 V)
20	–	I	Not used (power supply 5 V)
21	–	I	Not used (power supply 5 V)
22	–	I	Not used (power supply 5 V)
23	–	I	Not used (power supply 5 V)
24	–	I	Not used (power supply 5 V)
25	JOG2	I	Two-phase pulse signal input Input signal of a TA2OUT terminal is a period of "H", up count (clockwise) at rising edge of TA2IN terminal and down count (counterclockwise) at falling edge.
26	JOG1	I	
27	TOUCH	I	JOG touch sensor
28	JSCLK	O	Serial clock signal for JOG-FL
29	–	O	Not used (non connection)
30	J_SDO	O	Communication Serial data signal for JOG-FL
31	FLSDO	O	Communication Serial data signal for DATA-FL
32	–	I	Not used (non connection) For built-in flash memory updating
33	FLSCLK	O	Communication Serial clock signal for DATA-FL
34	–	I	Not used (non connection) For built-in flash memory updating
35	SDO	O	Communication Data out signal for MPU (MAIN ASSY)
36	SDI	I	Communication Data in signal for MPU (MAIN ASSY)
37	CLK	O	Communication Clock signal for MPU (MAIN ASSY)
38	XCS	O	Communication Chip select signal for MPU (MAIN ASSY)
39	–	O	Not used (non connection)
40	–	O	Not used (non connection)
41	–	I	Not used (pull up)
42	FLLAT	O	Communication Latch signal for DATA-FL
43	FLBK	O	Communication Blank signal for DATA-FL
44	JXSTB	O	Communication Latch signal for JOG-FL
45	JBK	O	Communication Blank signal for JOG-FL
46	XCE	I	Not used (pull up)
47	LED24	O	LED control for RELOOP/EXIT button 0 : Lights-out
48	LED23	O	LED control for REALTIME CUE OUT button 0 : Lights-out
49	LED22	O	LED control for PLAY/PAUSE button 0 : Lights-out
50	LED21	O	LED control for CUE button 0 : Lights-out

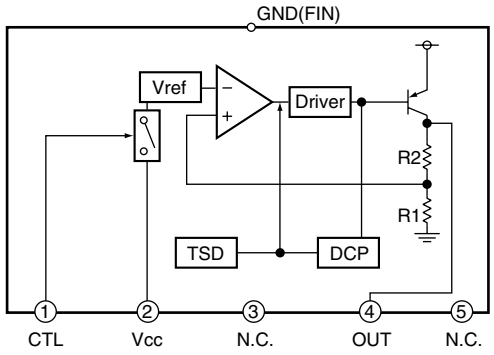
● **Pin Function**

No.	Pin Name	I/O	Pin Function
51	LED20	O	LED control for REV button 0 : Lights-out
52	LED19	O	LED control for REALTIME CUE IN button 0 : Lights-out
53	LED18	O	LED control for AUTO BEAT LOOP 8 button 0 : Lights-out
54	LED17	O	LED control for AUTO BEAT LOOP 4 button 0 : Lights-out
55	LED16	O	LED control for AUTO BEAT LOOP 2 button 0 : Lights-out
56	LED15	O	LED control for AUTO BEAT LOOP 1 button 0 : Lights-out
57	LED14	O	LED control for QUICK RETURN button 0 : Lights-out
58	LED13	O	LED control for JOG MODE button 0 : Lights-out
59	LED12	O	LED control for MASTER TEMPO button 0 : Lights-out
60	LED11	O	LED control for TEMPO button 0 : Lights-out
61	–	O	Not used (non connection) 0 : Lights-out
62	Vcc	–	Power supply 5 V
63	–	O	Not used (non connection) 0 : Lights-out
64	Vss	–	Ground
65	–	O	Not used (non connection) 0: Lights-out
66	–	O	Not used (non connection) 0: Lights-out
67	–	O	Not used (non connection) 0: Lights-out
68	–	O	Not used (non connection) 0: Lights-out
69	–	O	Not used (non connection) 0: Lights-out
70	–	O	Not used (non connection) 0: Lights-out
71	–	O	Not used (non connection) 0: Lights-out
72	–	O	Not used (non connection) 0: Lights-out
73	–	I	Not used (ground)
74	–	I	Not used (ground)
75	–	I	Not used (ground)
76	–	I	Not used (ground)
77	–	I	Not used (ground)
78	–	I	Not used (ground)
79	SW10	I	SW input (direct port) for RELOOP/EXIT button
80	SW09	I	SW input (direct port) for PLAY/PAUSE button
81	SW08	I	SW input (direct port) for CUE button
82	SW07	I	SW input (direct port) for REALTIME CUE OUT button
83	SW06	I	SW input (direct port) for REV button
84	SW05	I	SW input (direct port) for REALTIME CUE IN button
85	SW04	I	SW input (direct port) for AUTO BEAT LOOP 8 button
86	SW03	I	SW input (direct port) for AUTO BEAT LOOP 4 button
87	SW02	I	SW input (direct port) for AUTO BEAT LOOP 2 button
88	SW01	I	SW input (direct port) for AUTO BEAT LOOP 1 button
89	TEMPOR	I	SW input (A/D conversion port) for TEMPO SLIDER (2.5 V input)
90	TEMPO	I	SW input (A/D conversion port) for TEMPO SLIDER + direction: Vcc side, - direction: GND side
91	KEY0	I	SW input (A/D conversion port) for PLAY/CUE/TRACK SEARCH L/TRACK SEARCH R/SERCH L/SEARCH R button
92	KEY1	I	SW input (A/D conversion port) for FOLDER SEARCH +/FOLDER SEARCH -/QUICK RETURN button
93	KEY2	I	SW input (A/D conversion port) for CALL </CALL >/CUE DELETE/CUE MEMORY/TEXT MODE/TIME MODE button
94	–	I	Not used (power supply 5 V)
95	–	I	Not used (power supply 5 V)
96	AVss	–	Ground (for A/D conversion port)
97	MODEL	I	Power supply 5 V DVD destination seeting
98	VREF	–	Reference voltage (for A/D conversion port)
99	AVcc	–	Power supply 5 V (for A/D conversion port)
100	–	I	Power supply 5 V

BA50BC0WFP (SECB ASSY: IC57)

• Regulator IC (Built-in thermal shutdown protection, output variable type)

● Block Diagram



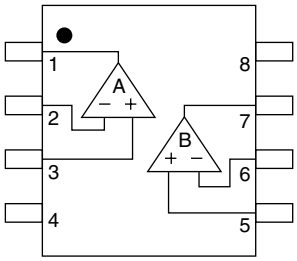
● Pin Function

No.	Pin Name	I/O	Pin Function
1	CTL	I	Output switch control
2	VCC	–	Power supply
3	N.C.	–	Non connection
4	OUT	O	Output
5	N.C.	–	Non connection
FIN	GND	–	Ground

NJM4558DX (JACK ASSY : IC801)

• DUAL OP-AMP IC (OP-AMP)

● Block Diagram



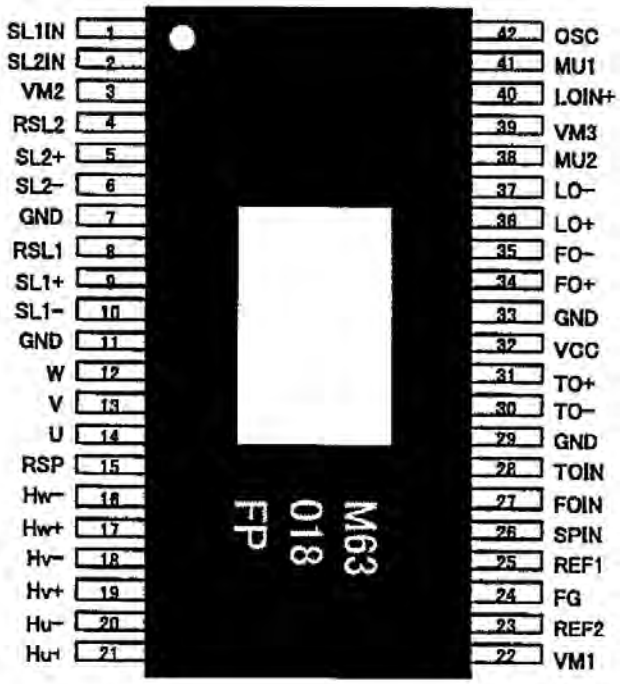
● Pin Function

No.	Pin Name	I/O	Pin Function
1	A OUTPUT	O	Output A
2	A -INPUT	I	Input A-
3	A +INPUT	I	Input A+
4	V-	–	Power supply -
5	B +INPUT	I	Input B+
6	B -INPUT	I	Input B-
7	B OUTPUT	O	Output B
8	V+	–	Power supply +

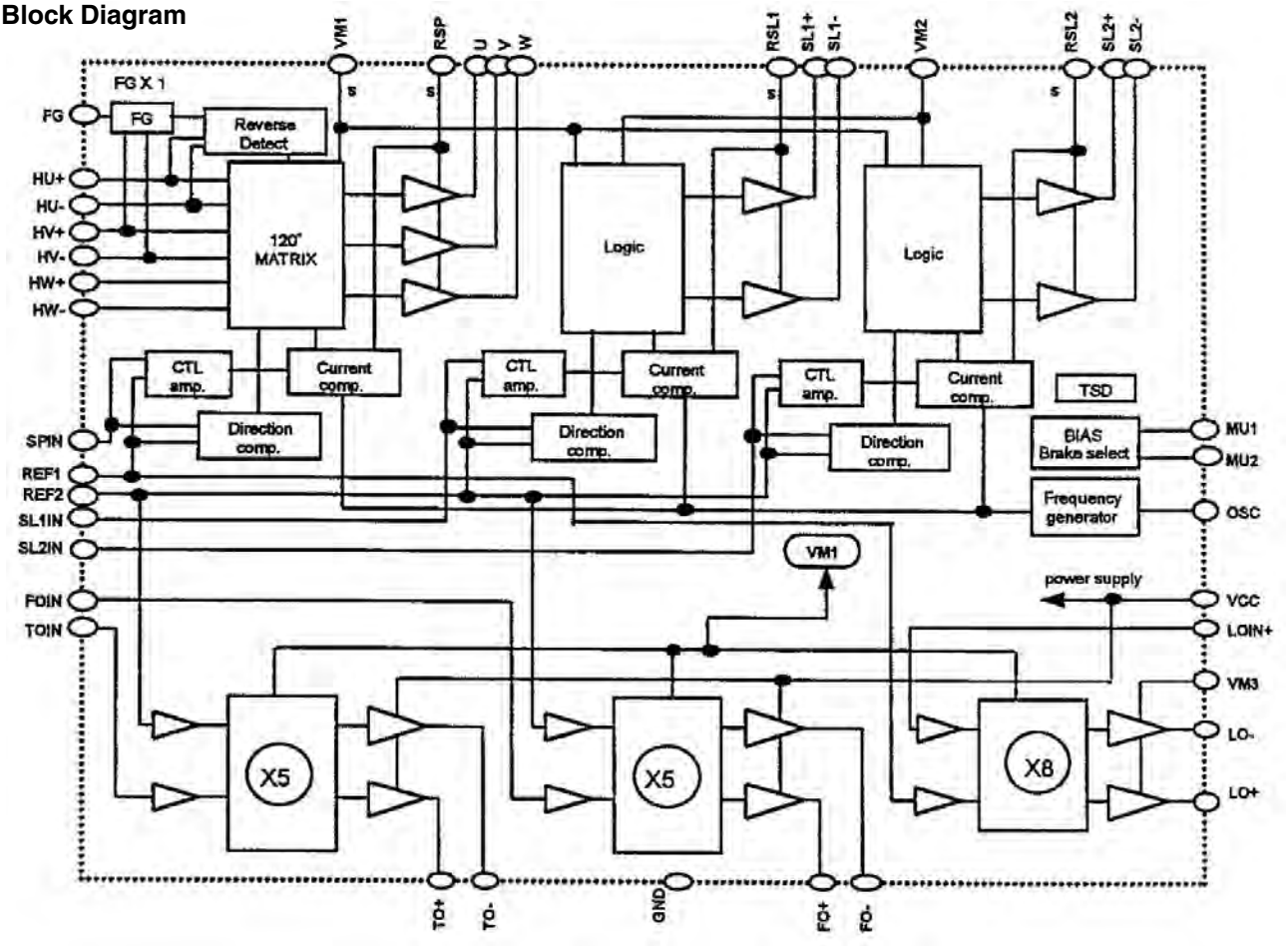
■ M63018FP (MAIN ASSY : IC102)

• Spindle Motor and 5ch Actuator Driver

● Pin Arrangement (Top view)



● Block Diagram



● **Pin Function**

TERMINAL	SYMBOL	TERMINAL FUNCTION	TERMINAL	SYMBOL	TERMINAL FUNCTION
1	SL1IN	Slide control voltage input 1	42	OSC	PWM carrier oscillation set
2	SL2IN	Slide control voltage input 2	41	MU1	mute / brake select terminal 1
3	VM2	Motor Power Supply 2 (for Slide)	40	LOIN+	Loading control input(+)
4	RSL2	Slide current sense 2	39	VM3	Power Supply3 (for Loading)
5	SL2+	Slide non-inverted output 2	38	MU2	mute / brake select terminal 2
6	SL2-	Slide inverted output 2	37	LO-	Loading inverted output
7	GND	GND	36	LO+	Loading non-inverted output
8	RSL1	Slide current sense 1	35	FO-	Focus inverted output
9	SL1+	Slide non-inverted output 1	34	FO+	Focus non-inverted output
10	SL1-	Slide inverted output 1	33	GND	GND
11	GND	GND	32	VCC	Power Supply (for FS ,TS)
12	W	Motor drive output W	31	TO+	Tracking non-inverted output
13	V	Motor drive output V	30	TO-	Tracking inverted output
14	U	Motor drive output U	29	GND	GND
15	RSP	Spindle current sense	28	TOIN	Tracking control voltage input
16	HW-	HW- sensor amp. input	27	FOIN	Focus control voltage input
17	HW+	HW+ sensor amp. input	26	SPIN	Spindle control voltage input
18	HV-	HV- sensor amp. input	25	REF1	Reference voltage input 1 (for Spindle,Loading)
19	HV+	HV+ sensor amp. input	24	FG	Frequency generator output
20	HU-	HU- sensor amp. input	23	REF2	Reference voltage input 2 (for Slide,Focus,Tracking)
21	HU+	HU+ sensor amp. input	22	VM1	Motor Power Supply 1 (for Spindle)

■ XC3S50-4VQG100C-K (MAIN ASSY : IC302)

• FPGA IC

● Pin Arrangement (Top view)

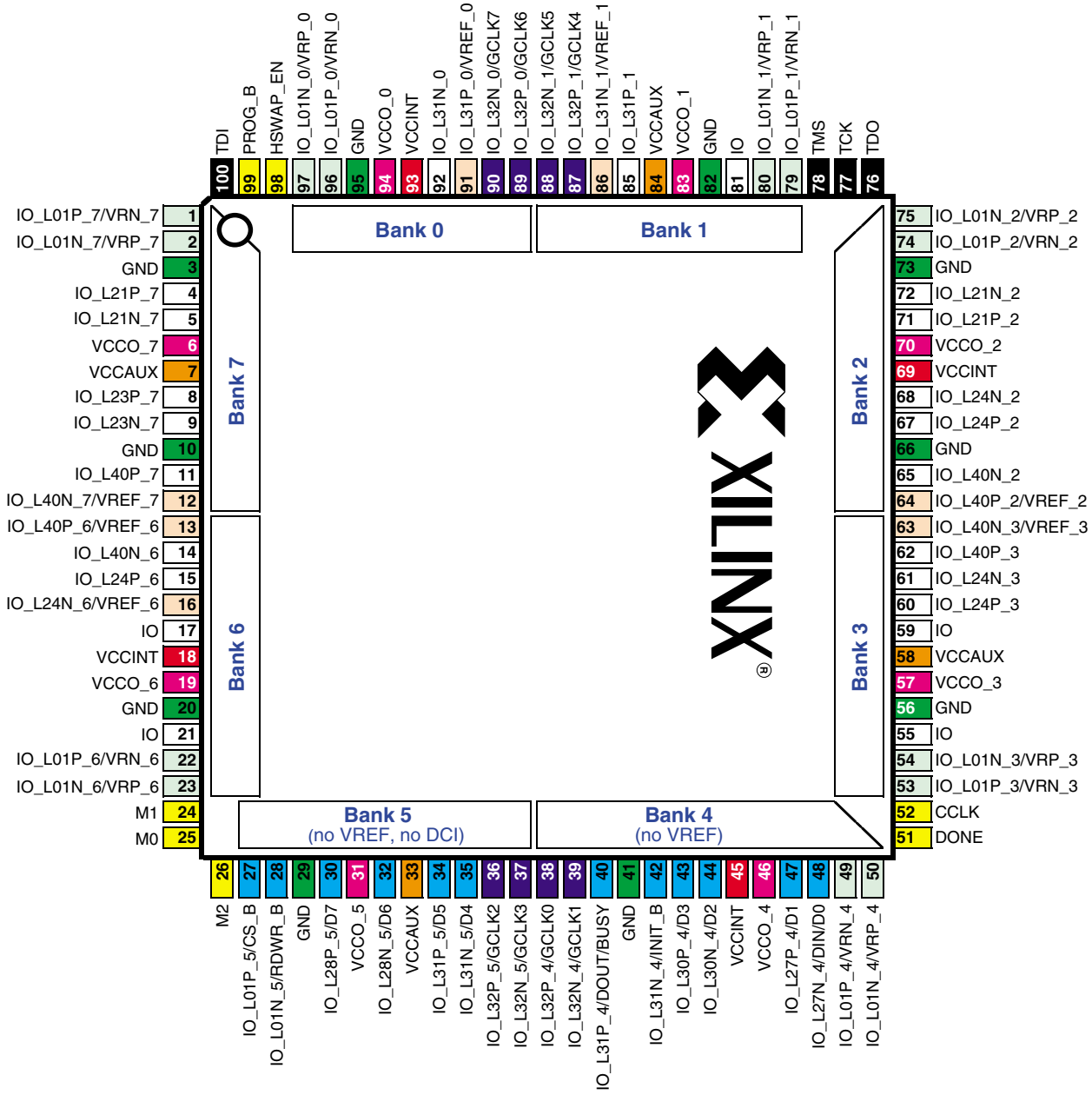
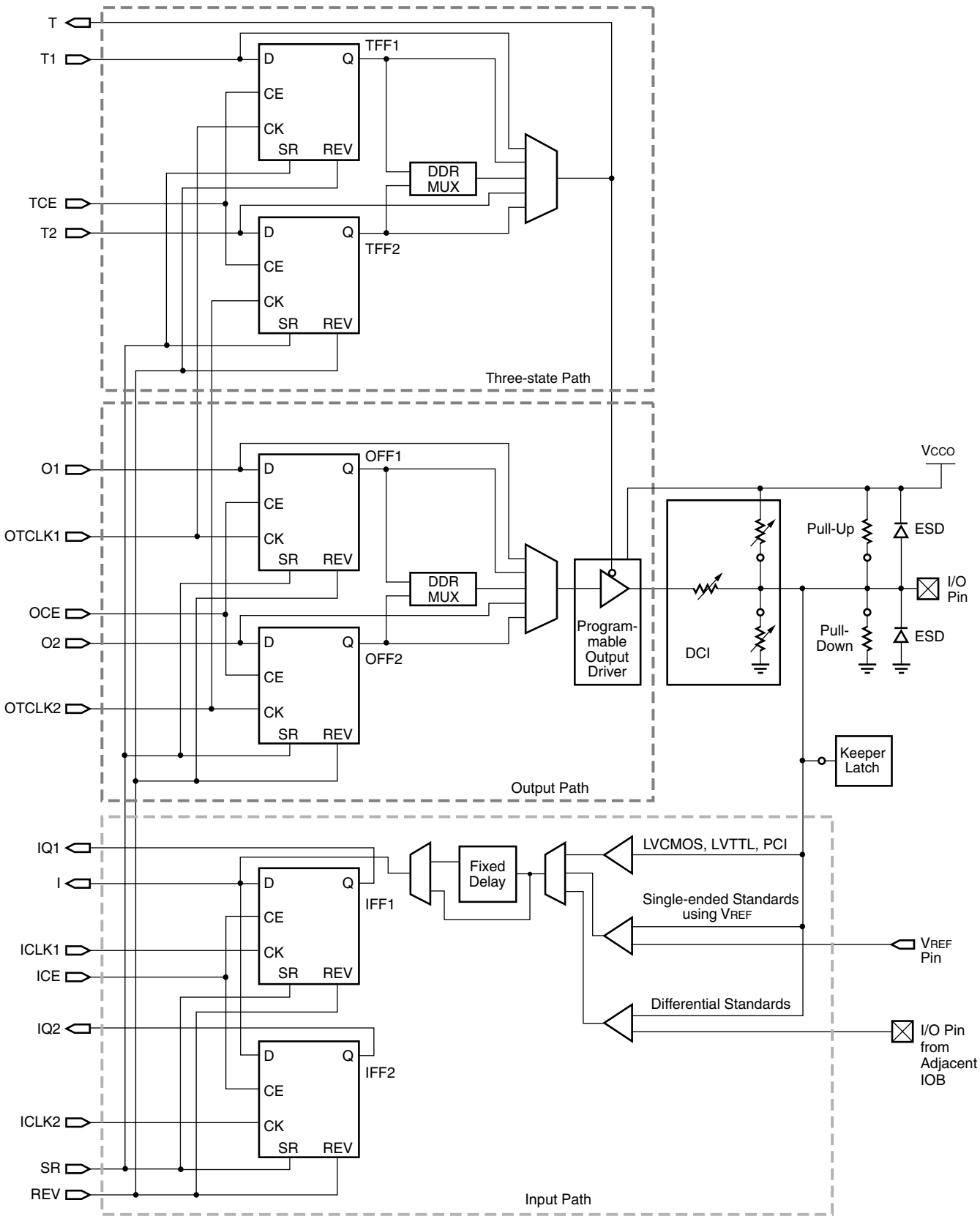


Figure 5 : **VQ100 Package Footprint (top view). Note pin 1 indicator in top-left corner and logo orientation.**

22	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possibl user I/O	7	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	8	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	10	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

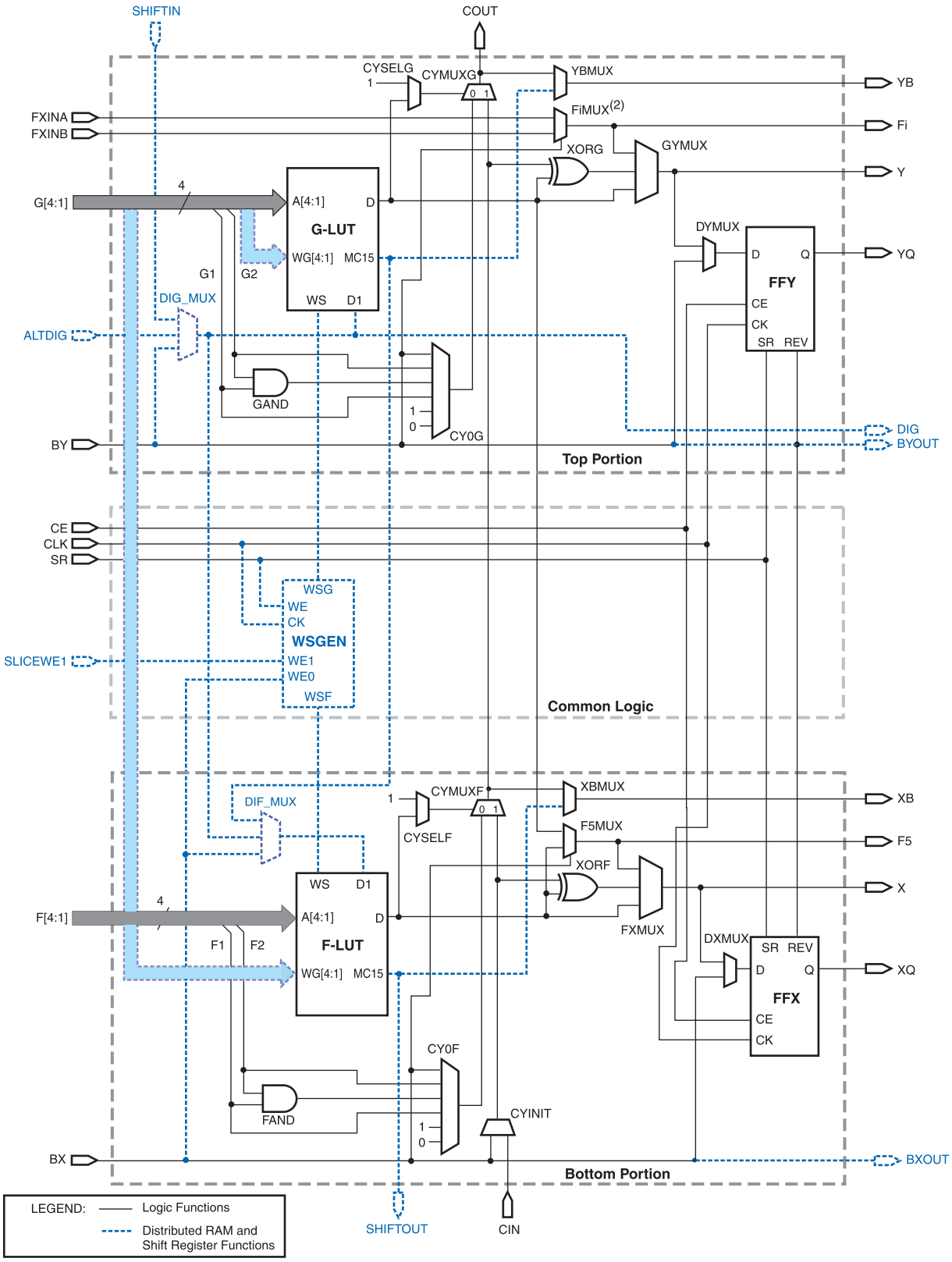
● Block Diagram



Note : All IOB signals communicating with the FPGA's internal logic have the option of inverting polarity.

Figure 1: **Simplified IOB Diagram**

● Block Diagram



Notes:

1. Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
2. The index i can be 6, 7, or 8, depending on the slice. In this position, the upper right-hand slice has an F8MUX, and the upper left-hand slice has an F7MUX. The lower right-hand and left-hand slices both have an F6MUX.

Figure 6 : **Simplified Diagram of the Left-Hand SLICEM**

■ K4S641632K-UC75 (MAIN ASSY : IC303)

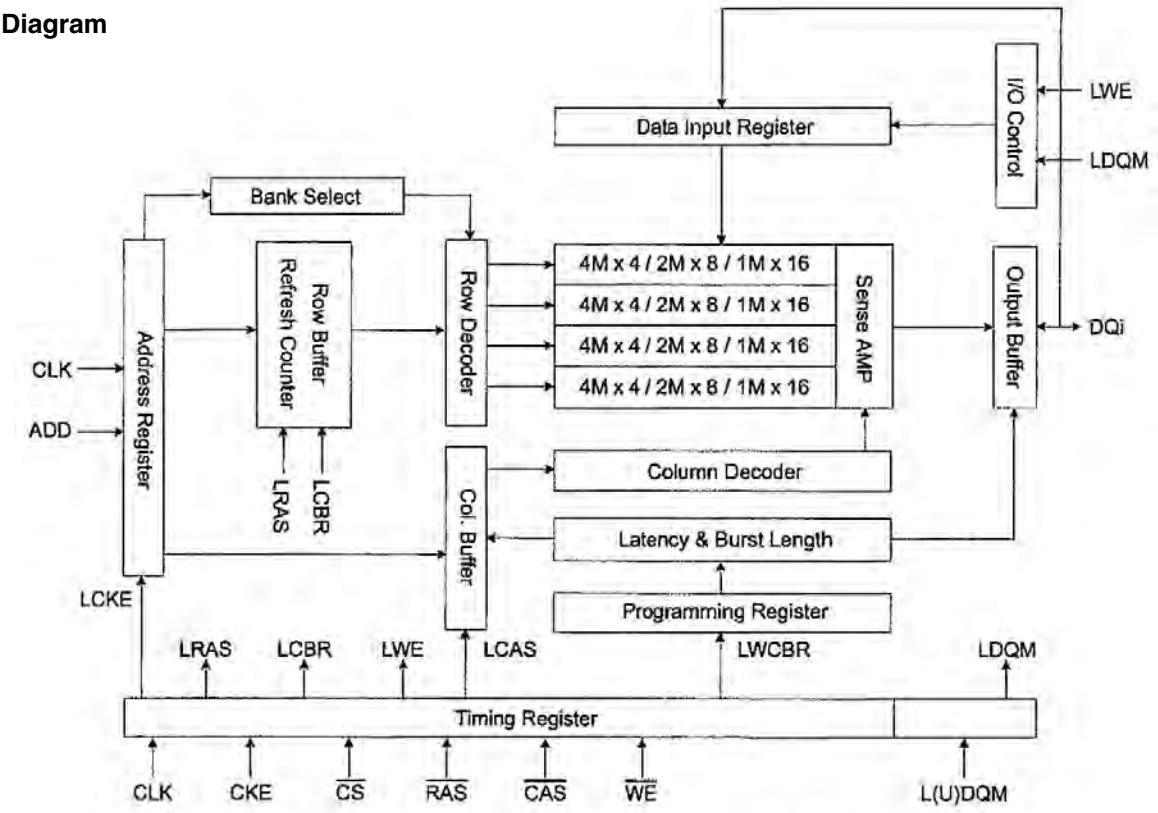
• SDRAM (64Mbit)

● Pin Arrangement (Top view)

x16	x8	x4			x4	x8	x16
VDD	VDD	VDD	1	54	VSS	VSS	VSS
DQ0	DQ0	N.C	2	53	N.C	DQ7	DQ15
VDDQ	VDDQ	VDDQ	3	52	VSSQ	VSSQ	VSSQ
DQ1	N.C	N.C	4	51	N.C	N.C	DQ14
DQ2	DQ1	DQ0	5	50	DQ3	DQ6	DQ13
VSSQ	VSSQ	VSSQ	6	49	VDDQ	VDDQ	VDDQ
DQ3	N.C	N.C	7	48	N.C	N.C	DQ12
DQ4	DQ2	N.C	8	47	N.C	DQ5	DQ11
VDDQ	VDDQ	VDDQ	9	46	VSSQ	VSSQ	VSSQ
DQ5	N.C	N.C	10	45	N.C	N.C	DQ10
DQ6	DQ3	DQ1	11	44	DQ2	DQ4	DQ9
VSSQ	VSSQ	VSSQ	12	43	VDDQ	VDDQ	VDDQ
DQ7	N.C	N.C	13	42	N.C	N.C	DQ8
VDD	VDD	VDD	14	41	VSS	VSS	VSS
LDQM	N.C	N.C	15	40	N.C/RFU	N.C/RFU	N.C/RFU
WE	WE	WE	16	39	DQM	DQM	UDQM
CAS	CAS	CAS	17	38	CLK	CLK	CLK
RAS	RAS	RAS	18	37	CKE	CKE	CKE
CS	CS	CS	19	36	N.C	N.C	N.C
BA0	BA0	BA0	20	35	A11	A11	A11
BA1	BA1	BA1	21	34	A9	A9	A9
A10/AP	A10/AP	A10/AP	22	33	A8	A8	A8
A0	A0	A0	23	32	A7	A7	A7
A1	A1	A1	24	31	A6	A6	A6
A2	A2	A2	25	30	A5	A5	A5
A3	A3	A3	26	29	A4	A4	A4
VDD	VDD	VDD	27	28	VSS	VSS	VSS

54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

● Block Diagram



* Samsung Electronics reserves the right to change products or specification without notice.

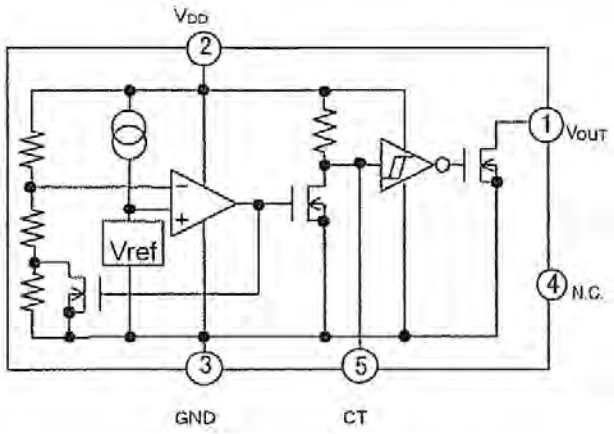
● Pin Function

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, Column address : CA_0 ~ CA_9
BA_0 ~ BA_1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ_0 ~ X_{15}	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

■ BU4230G (MAIN ASSY : IC304)

• RESET IC

● Block Diagram



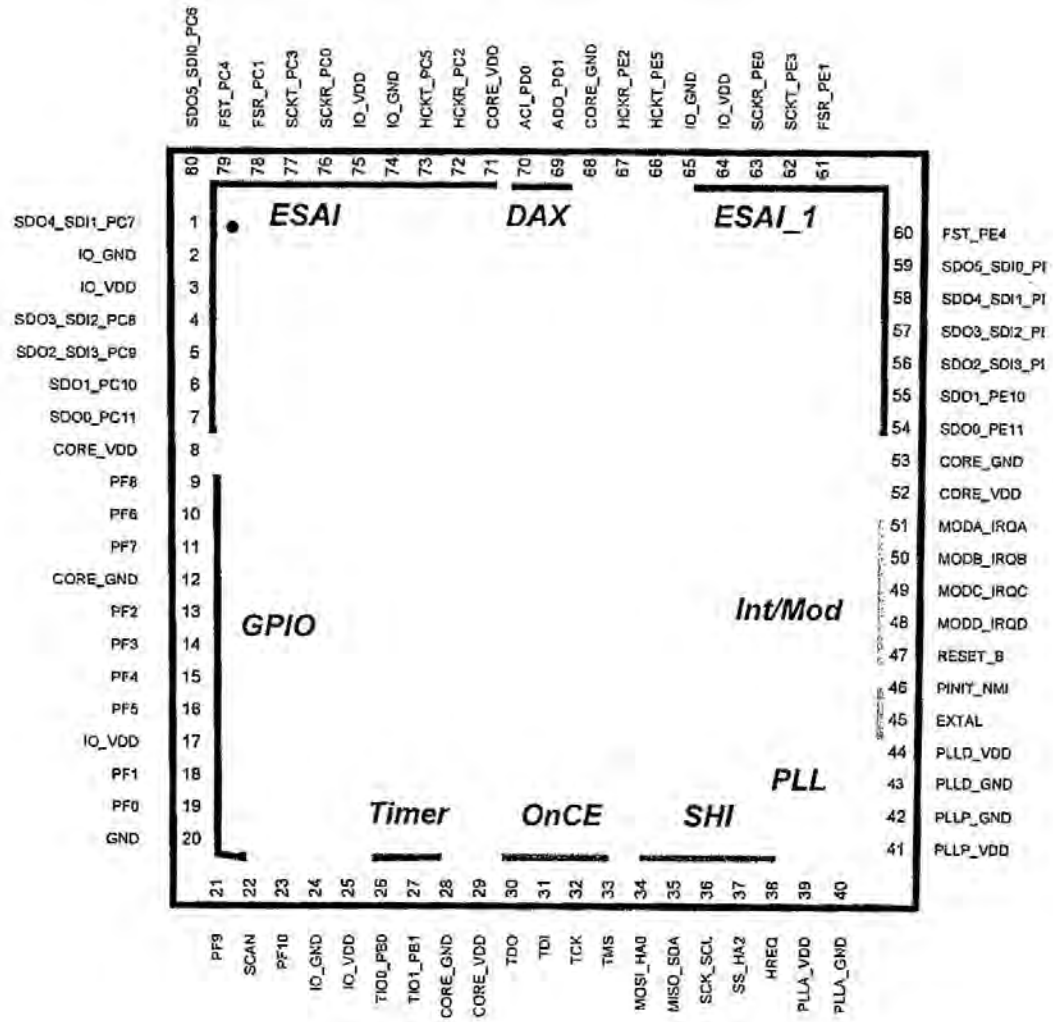
● Pin Function

Pin Number	Pin Name
1	VOUT
2	VDD
3	GND
4	N.C.
5	CT

■ DSPC56371AF180 (MAIN ASSY : IC701)

• DSP IC

● **Pin Arrangement (Top view)**



● **Pin Function**

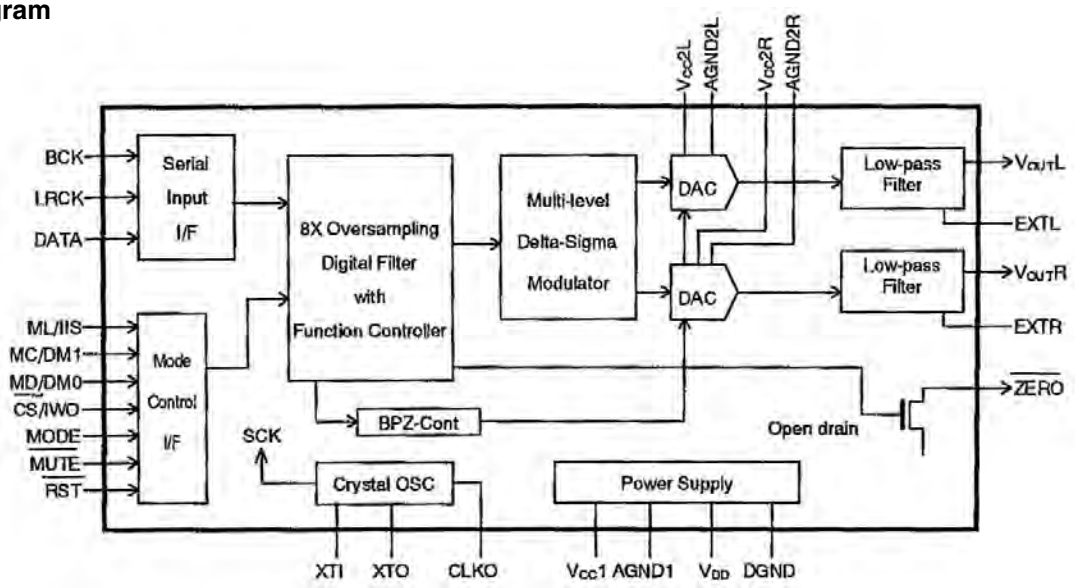
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	SDO4_SDM_PC7	21	PF9	41	PLLP_VDD	61	FSR_PE1
2	IO_GND	22	SCAN	42	PLLP_GND	62	SCKT_PE3
3	IO_VDD	23	PF10	43	PLLD_GND	63	SCKR_PE0
4	SDO3_SDI2_PC8	24	IO_GND	44	PLLD_VDD	64	IO_VDD
5	SDO2_SDI3_PC9	25	IO_VDD	45	EXTAL	65	IO_GND
6	SDO1_PC10	26	TI0_PB0	46	PINIT_NMI	66	HCKT_PE5
7	SDO0_PC11	27	TI0_PB1	47	RESET_B	67	HCKR_PE2
8	CORE_VDD	28	CORE_GND	48	MODD_IRQD	68	CORE_GND
9	PF8	29	CORE_VDD	49	MODC_IRQC	69	ADO_PD1
10	PF6	30	TDO	50	MODB_IRQB	70	ADI_PD0
11	PF7	31	TDI	51	MODA_IRQA	71	CORE_VDD
12	CORE_GND	32	TCK	52	CORE_VDD	72	HCKR_PC2
13	PF2	33	TMS	53	CORE_GND	73	HCKT2_PC5
14	PF3	34	MOSI_HA0	54	SDO0_PE11	74	IO_GND
15	PF4	35	MISO_SDA	55	SDO1_PE10	75	IO_VDD
16	PF5	36	SCK_SCL	56	SDO2_SDI3_PE9	76	SCKR_PC0
17	IO_VDD	37	SS_HA2	57	SDO3_SDI2_PW8	77	SCKT_PC3
18	PF1	38	HREQ	58	SDO4_SDI1_PE7	78	FSR_PC1
19	PF0	39	PLLA_VDD	59	SDO5_SD10_PE6	79	FST_PC4
20	GND	40	PLLA_GND	60	FST_PE4	80	SDO5_SDI10_PC6

■ PE8001A (MAIN ASSY : IC702)

• DAC IC

● Pin Arrangement (Top view)

● Block Diagram



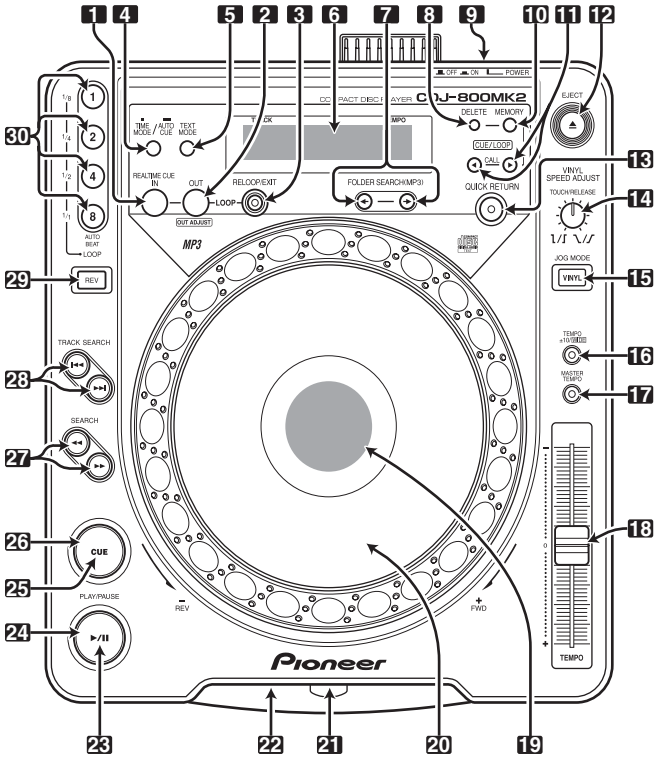
● Pin Function

PIN	NAME	I/O	DESCRIPTIONS
1	LRCK	IN	LRCK Clock Input (f_S). (1)
2	DATA	IN	Serial Audio Data Input. (1)
3	BCK	IN	Bit Clock Input for Serial Audio Data. (1)
4	CLKO	OUT	Buffered Output of System Clock.
5	XTI	IN	Oscillator Input / External Clock Input.
6	XTO	OUT	Oscillator Output.
7	DGND	-	Digital Ground.
8	V_{DD}	-	Digital Power, + 5 V
9	$V_{CC}2R$	-	Analog Power, + 5 V
10	AGND2R	-	Analog Ground.
11	EXTR	OUT	Rch, Common Pin of Analog Output Amp.
12	NC	-	Non Connection.
13	$V_{OUT}R$	OUT	Rch, Analog Voltage Output of Audio signal.
14	AGND1	-	Analog Ground.
15	$V_{CC}1$	-	Analog Power, + 5 V
16	$V_{OUT}L$	OUT	Lch, Analog Voltage Output of Audio signal.
17	NC	-	Non Connection.
18	EXTL	OUT	Lch, Common Pin of Analog Output Amp
19	AGND2L	-	Analog Ground.
20	$V_{CC}2L$	-	Analog Power, + 5V
21	$\overline{ZERO}$	OUT	Zero Data Flag.
22	$\overline{RST}$	IN	Reset. When this pin is LOW, the DF & modulators are held in reset. (2)
23	$\overline{CS}$ / IWO	IN	Chip Select / Input format selection. (3)
24	MODE	IN	Mode Control Select. (H: Software, L: Hardware) (2)
25	$\overline{MUTE}$	IN	Mute Control. (2)
26	MD / DM0	IN	Mode Control, Data / De-emphasis selection 1. (2)
27	MC / DM1	IN	Mode Control, BCK / De-emphasis selection 2. (2)
28	ML / IIS	IN	Mode Control, WDCK / Input format selection. (2)

8pt:

(1) Pins 1, 2, 3: Schmitt-trigger input.
(2) Pins 22, 24, 25, 26, 27, 28: Schmitt-trigger input with internal pull-up.
(3) Pin 23: Schmitt-trigger input with internal pull-down.

8. PANEL FACILITIES
8.1 PANEL FACILITES



1. LOOP IN/REALTIME CUE button/indicator
Realtime cue
Loop-in point input

2. LOOP OUT (OUT ADJUST) button/indicator
Loop-out point input
Loop-out point adjust

3. RELOOP/EXIT button/indicator

4. TIME MODE/AUTO CUE button
TIME MODE:
Eachtime the button is pressed, the display's time display alternates between the current elapsed play time and the remaining play time (**REMAIN**).
When playing MP3, the **REMAIN** time may not display immediately, depending on the track.
• The current **TIME MODE** setting is retained in memory even when the power is turned off.
AUTO CUE:
When the button is held depressed for 1 second or more, the AUTO CUE mode is alternately enabled and disabled.
When the button is held depressed for 5 seconds or more, the AUTO CUE level is toggled.
• The current AUTO CUE on/off and AUTO CUE level settings are retained in memory even when power is turned off.

5. TEXT MODE button
When this button is pressed, the TEXT display mode is enabled, and each additional time the button is pressed, the display alternates between track name, album name, and artist name.
• To set to time display, press the **TIME MODE/AUTO CUE** button.

6. Display

7. FOLDER SEARCH buttons (← , →)
During MP3 playback, layered CD-ROM folder search will be performed in the designated direction.

8. CUE/LOOP DELETE button
Use to delete cue points and loop points from internal memory.

9. POWER OFF ▙/ON ▁ switch
This switch is located on the rear panel of the unit.

10. CUE/LOOP MEMORY button
Use to record cue points and loop points to internal memory .

11.CUE/LOOP CALL buttons (◄, ►)
Use to call cue points and loop points recorded in internal memory.

12.EJECT button (▲)
When button is pressed, disc rotation stops and disc is ejected fromport.

13.QUICK RETURN button/indicator
If this switch is set to ON when the JOG MODE is set to [**VINYL**], pressing the surface of the Jog dial will cause play to return quickly to the cue point.

14.VINYL SPEED ADJUST TOUCH/RELEASE dial
This dial control is used to adjust the deceleration speed from play to full stop when the JOG MODE is set to [**VINYL**] and the jog dial surface is pressed, and also the acceleration speed from full stop to play when the user's finger is removed from the surface of the jog dial.

15.JOG MODE VINYL button/indicator
VINYL mode: The button indicator lights. When the surface of the jog dial is pressed during playback, play stops, and if the jog dial is then rotated, sound is produced in accordance with the degree of rotation.
• The currently set jog mode is stored in memory even when power is turned off.
CDJ mode: The above action does not occur when the jog dial is pressed.

16.TEMPO control range selector button/indicator (TEMPO ±10/WIDE)
Each time the button is pressed, the variable range of the **TEMPO** adjust slider alternates (±10 %/WIDE). The button lights when [**WIDE**] is selected.
• When playing CDs, the variable during [**WIDE**] selection is ±100 %; when playing MP3, the variable range with [**WIDE**] is ±16 %.

17.MASTER TEMPO button/indicator
When pressed, the master tempo function alter nates ON/OFF.

18. TEMPO adjust slider
When moved toward the user (+ front), the track tempo increases, and when moved away from the user (– rear), the tempo decreases.

19. Jog dial display

20. Jog dial (+FWD/–REV)

21. Disc loading slot

22. Forced eject hole

23. Play/pause indicator (►/❚❚)
Lights during playback, and flashes during pause mode.

24. PLAY/PAUSE button (►/❚❚)

25. CUE indicator
Lights when a Cue point is set. Flashes in pause mode.

26. CUE button
Cue point setting
Back cue
Cue point sampler

27. SEARCH buttons (◄◄, ►►)

28. TRACK SEARCH buttons (I◄◄, ►►I)

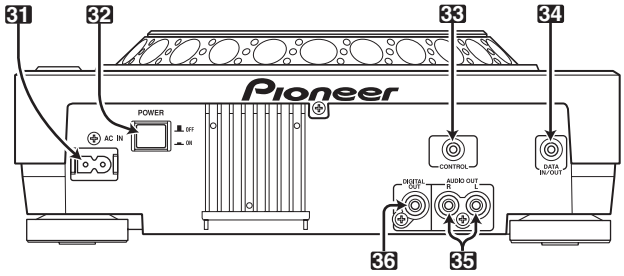
29. Reverse button / indicator (REV)

When this button is pressed, its indicator lights and the unit is set to reverse play.

30. AUTO BEAT LOOP buttons / indicators (1, 2, 4, 8) (1/8, 1/4, 1/2, 1/1)

When this button is pressed, auto loop play is performed based on the track's BPM (1 beat, 2 beats, 4 beats or 8 beats).
When a loop has been set manually, the button operates as a loop shortening button. (**1**=1/8, **2**=1/4, **4**=1/2, **8**=1/1).

Rear Panel



31. AC inlet (AC IN)

Use the accessory power cord to connect this inlet to a standard AC power outlet.

32. POWER ■OFF/▂ON switch

33. CONTROL connector

When the accessory control cord is used to connect this connector to the corresponding CONTROL connector on a Pioneer DJ mixer, the DJ mixer can be used to control the CD player for fader start play and back cue.
Also, by connecting this connector to the CONTROL connector on another Pioneer DJ CD player, automatic relay play can be performed.

34. DATA IN/OUT connector

When a commercially available miniplug cord (or the accessory control cord) is used to connect this jack to the same jack on another CDJ-800MK2, recorded data such as cue points and loop points can be copied from one player to the other.

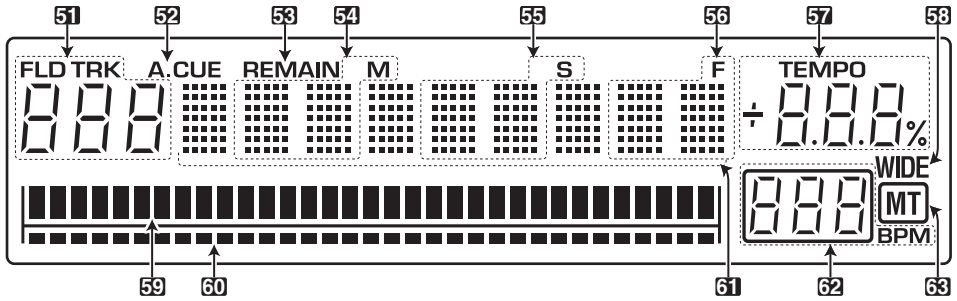
35. AUDIO OUT L, R connectors

RCA-type analog audio output jacks.

36. DIGITAL OUT connector

RCA type coaxial digital output connectors used to connect a DJ mixer or AV amplifier, CD player, etc., equipped with digital input connectors. The digital outputs here support all DJ and other functions, but only audio data is output (without subcodes; CD graphics are not supported).

Display Section



51. Track number/folder number display (TRK/FLD)
When playing an audio CD, the [**TRK**] indicator lights, and the two-digit track number appears (01 to 99).
When playing MP3, [**TRK**] lights and the track number is displayed in three digits (01 to 999). During folder search, the [**FLD**] indicator lights, and a two-digit folder number is displayed (00 to 99).

52. Auto cue indicator (A.CUE)
Lights when auto cue is ON.

53. REMAIN indicator
This indicator lights to indicate that track's remaining time is being displayed.

54. Time (minutes) display (M)

55. Time (seconds) display (S)

56. Frame display (F)
Seventy-five frames equal one second.

57. TEMPO display
Displays change in playing speed (tempo) caused by movement of the **TEMPO** adjust slider.

58. Tempo control range display (WIDE)
Lights when **TEMPO ±10/WIDE** button is set to [**WIDE**].

59. Playing address display
Toprovided a quick grasp of the current track's elapsed time and remaining playing time, the entire track is shown as a bar graph scaled over the entire width of the display.
- During elapsed time display, the bar graph's indicator segments turn on from left to right.
- During remaining time display, the bar graph indicator segments turn off from left to right.
- When a track has less than 30 seconds of remaining play time, the graph flashes slowly; when less than 15 seconds remain, the flashing becomes quicker.

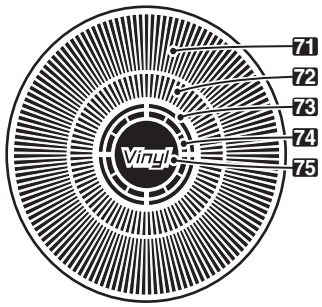
60. Memory point display
If cue memory or loop memory has been recorded in the currently playing track, its relative starting position is displayed here.

61. Dot matrix display (7x5 dots by 9 segments)
The dot matrix is used to display TEXT, guides and other information. Text up to 48 characters can be displayed (text longer than 8 characters is scrolled).

62. BPM display (0 to 360 BPM)
This display shows the Beats-Per-Minute (BPM) of the currently playing track (detection range 70 to 180 BPM). The automatic BPM counter may be unable to compute the correct BPM for some tracks.

63. Master tempo indicator (MT)
Lights when the master tempo function is ON.

Jog dial display



71. Operation display
This display shows the relative playing position, with one revolution equivalent to 135 frames. During playback, the display rotates, and it stops during pause mode.

72. Cue point position indicator
Indicates position of cue points.

73. Audio memory status indicator
This indicator flashes during audio memory write, and lights when writing has been sufficiently completed. When the indicator is flashing, it may not be possible to record real time cue points. The indicato ralso flashes when memory insufficiency occurs due to scratch operation.

74. Jog touch detection indicator
In VINYL mode, this indicator lights to indicate that the jog dial surface has been touched.

75. VINYL mode indicator
Lights during VINYL mode.

A

B

C

D

E

F

■ Lubricants and Glues list

Name	Lubricants and Glues No.	Remark
Dyefree	GEM1036 (ZLX-ME413A)	Refer to "2.4 SLOT-IN MECHANISM SECTION"
Grease	GYA1001 (ZLB-PN397B)	Refer to "2.3 CONTROL PANEL SECTION", "2.4 SLOT-IN MECHANISM SECTION"
Grease	GYA1007 (ZLB-PN348P)	Refer to "2.4 SLOT-IN MECHANISM SECTION", "2.3 CONTROL PANEL SECTION"

■ Cleaning

• Before shipping out the product, be sure to clean the following positions by using the prescribed cleaning tools:

Position to be cleaned	Cleaning tools	Remark
Pickup leneses	Cleaning liquid : GEM1004	Refer to "2.4 SLOT-IN MECHANISM SECTION" , "7.1.5 DISASSEMBLY SECTION".
	Cleaning paper : GED-008	